



arm

Implementing debug and trace access through functional I/O

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Agenda

Debug and trace access limitations

A new approach

- Protocol based
- Bare metal vs mission mode
- Shared vs dedicated interface controller

Securing access

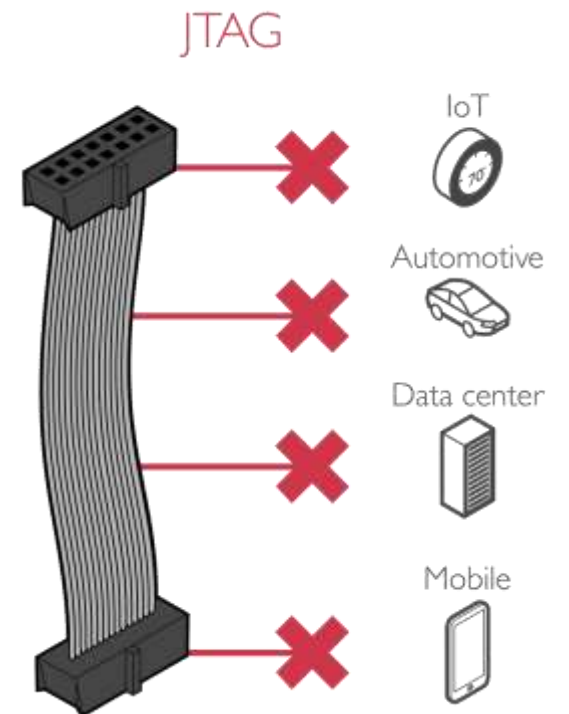
End-to-end solution

Limitations of JTAG-based access

Today's debug access over JTAG poses a number of practical challenges.

Visibility is increasingly being constrained by insufficient bandwidth.

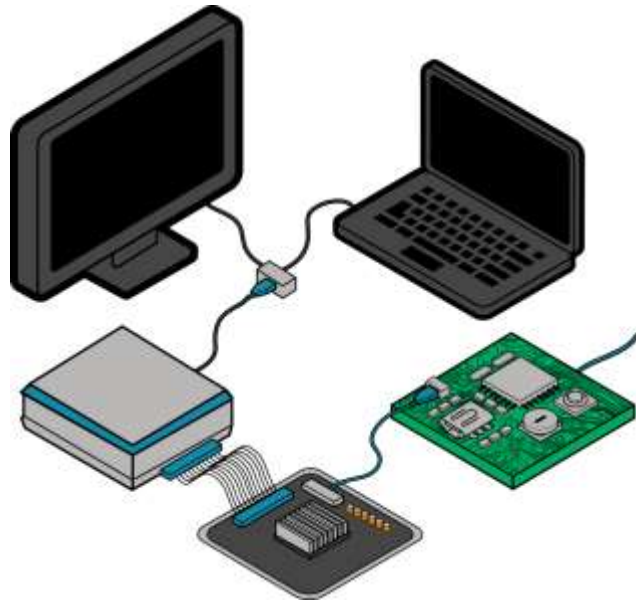
A new approach is required to provide sufficient visibility and bandwidth from silicon bring-up to in-field deployment.



Moving to protocol-based debug

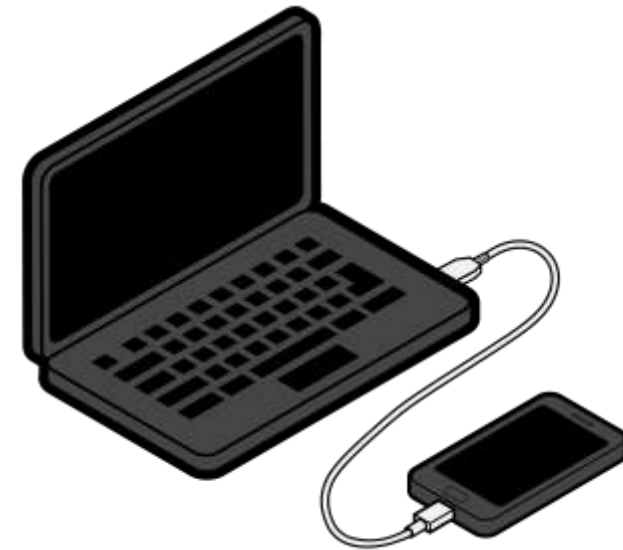
Today

Typically restricted to lab environment



Future

Access over arbitrary existing interface enables debug through product lifespan



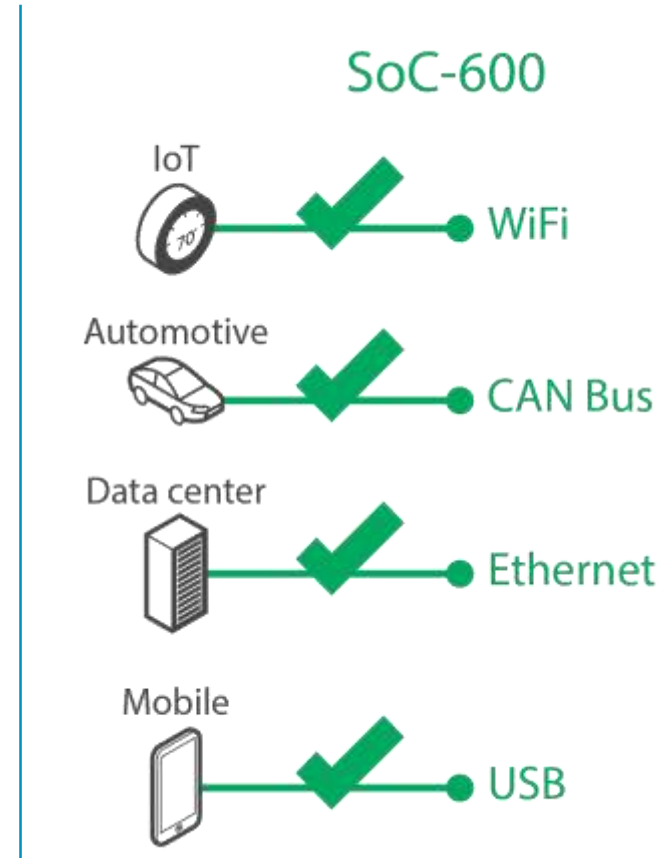
CoreSight SoC-600 – enabling debug throughout the product lifespan

Removes reliance on JTAG

- Better visibility through increased bandwidth
- Debug throughout product lifespan
- Remote debug reduces cost of ownership

Benefits include

- In-field debug, while device operating in its intended environment
- Remote debug sessions (e.g. data center, car, IoT node)
- More bandwidth translates to faster fault identification
 - E.g. debug and trace over same link
- IO cost savings

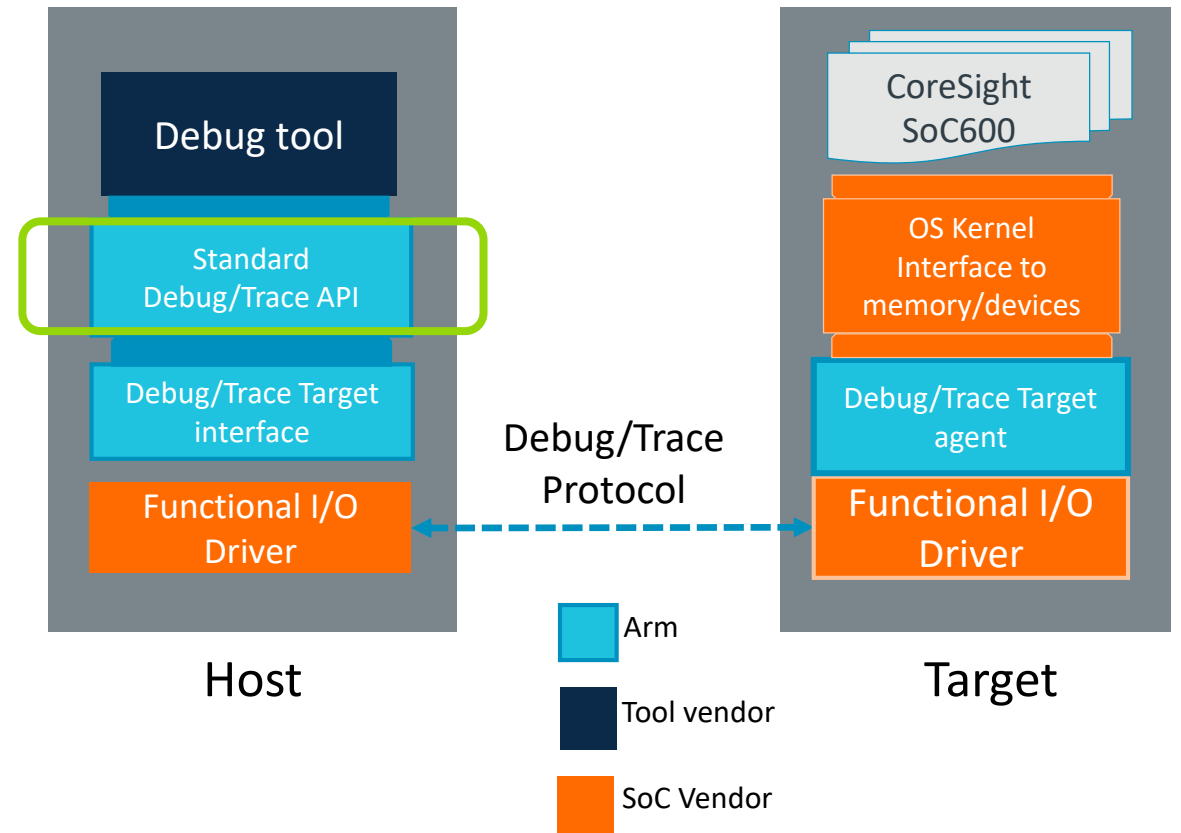


Standard API – one API for all tools

Standard API used by debug/analysis tools to

- Configure the target
- Debug the target
- Receive trace from the target

This abstracts the underlying protocols and transport.

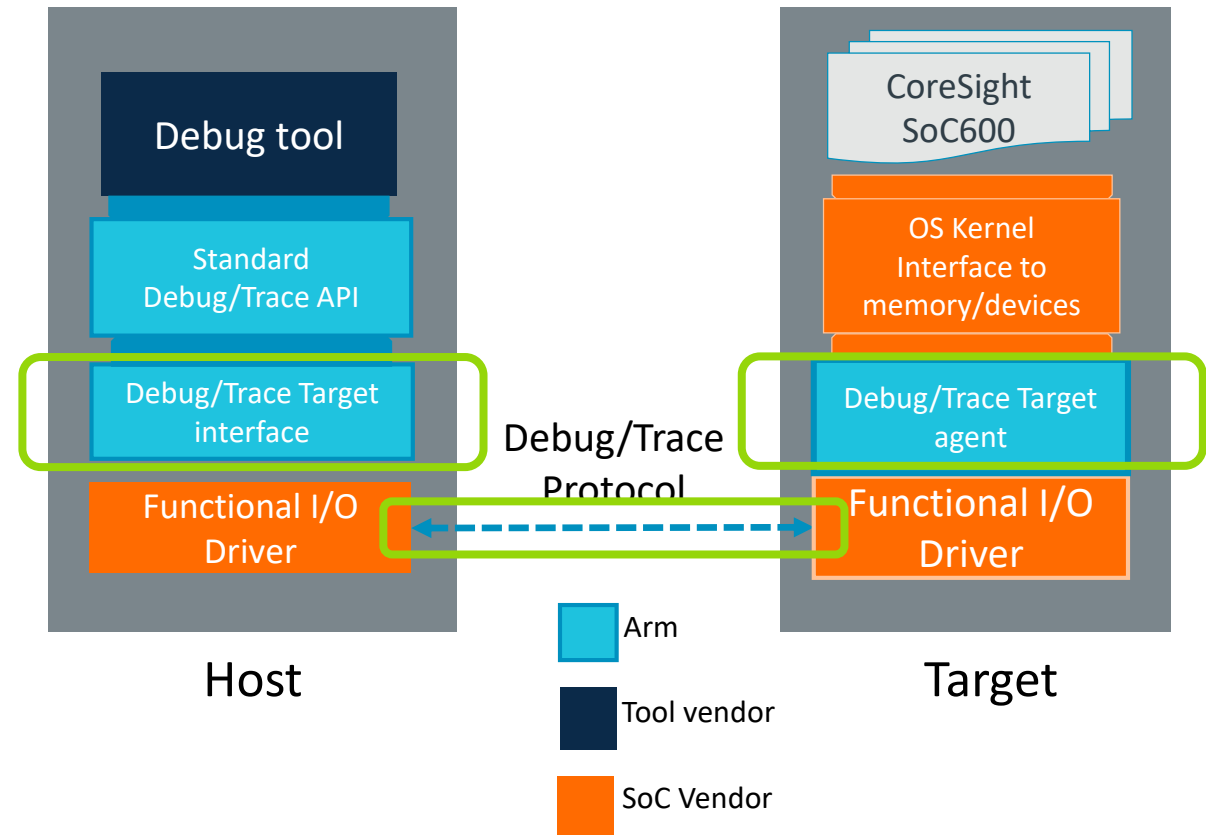


Reference protocol spec/implementation

Arm to provide a protocol specification and host/target reference software implementations.

CoreSight Wire Protocol - CSWP

Reference code will be freely available.



A practical approach balancing cost, intrusiveness and performance (part 1)

Lowest silicon cost

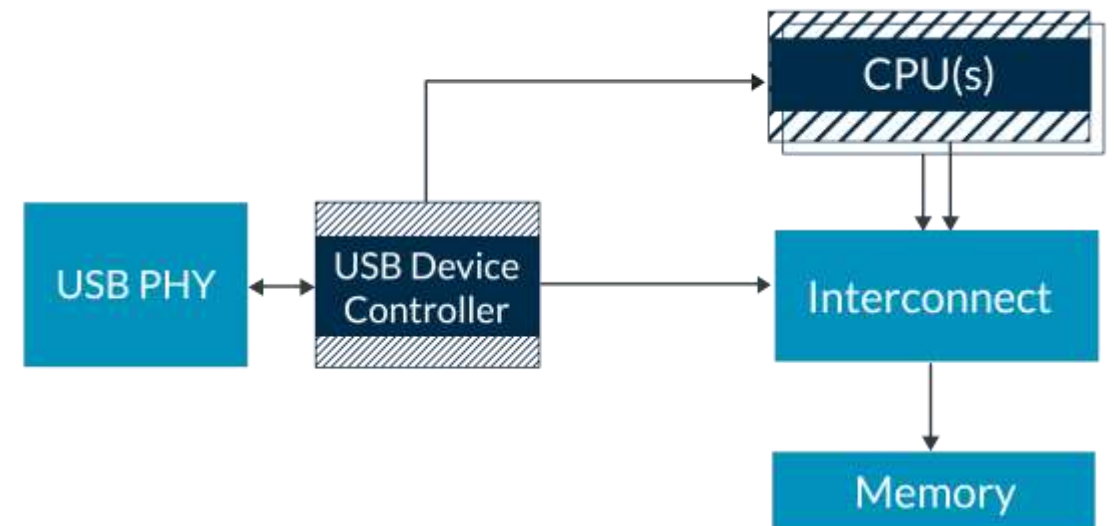
- No additional dedicated resources needed

Intrusive

- Protocol and link run by same CPU being debugged

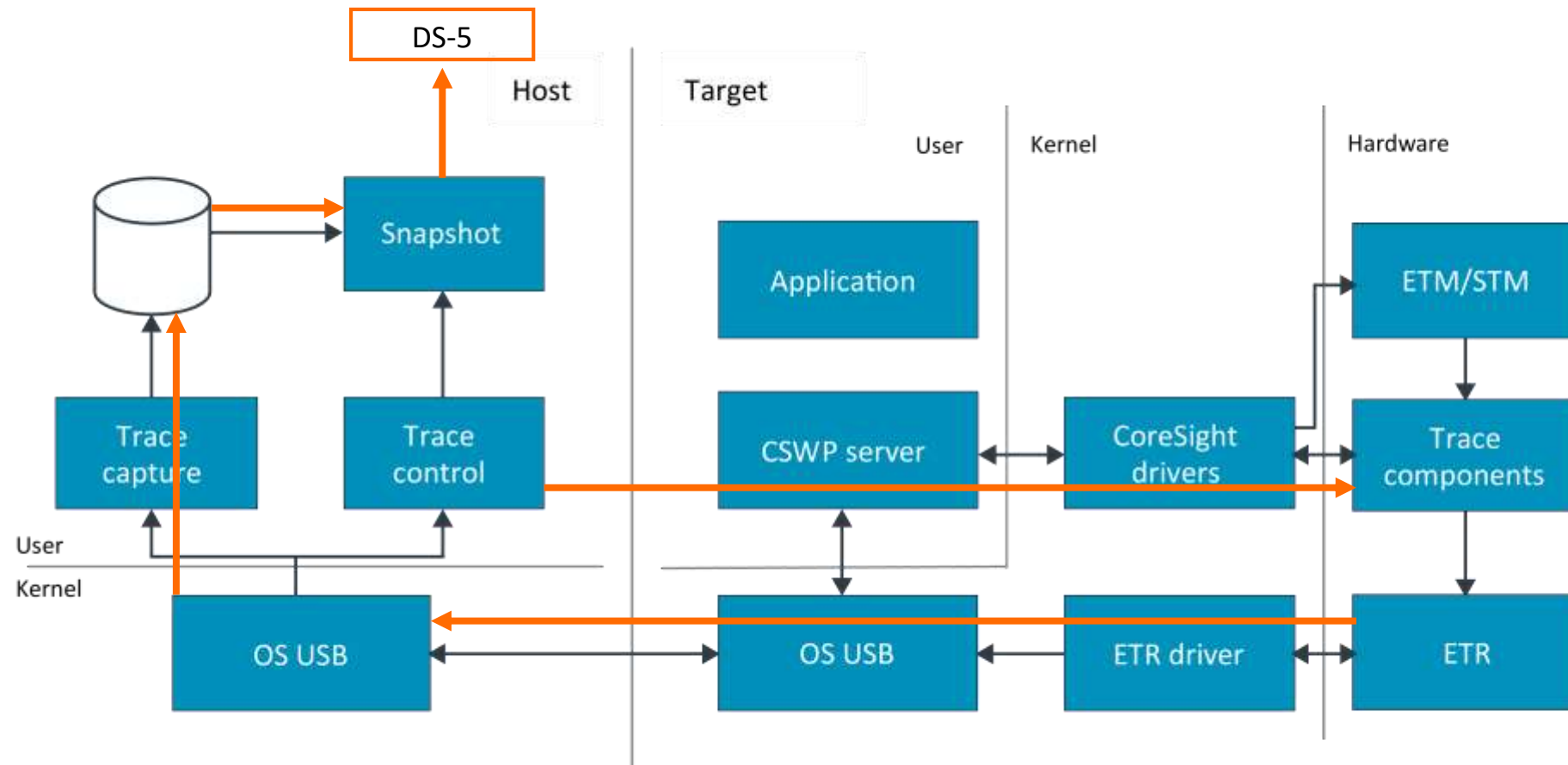
Bare-metal debug not supported

- Link owned by same target CPU



Legend
■ Shared

Mission Mode - software view

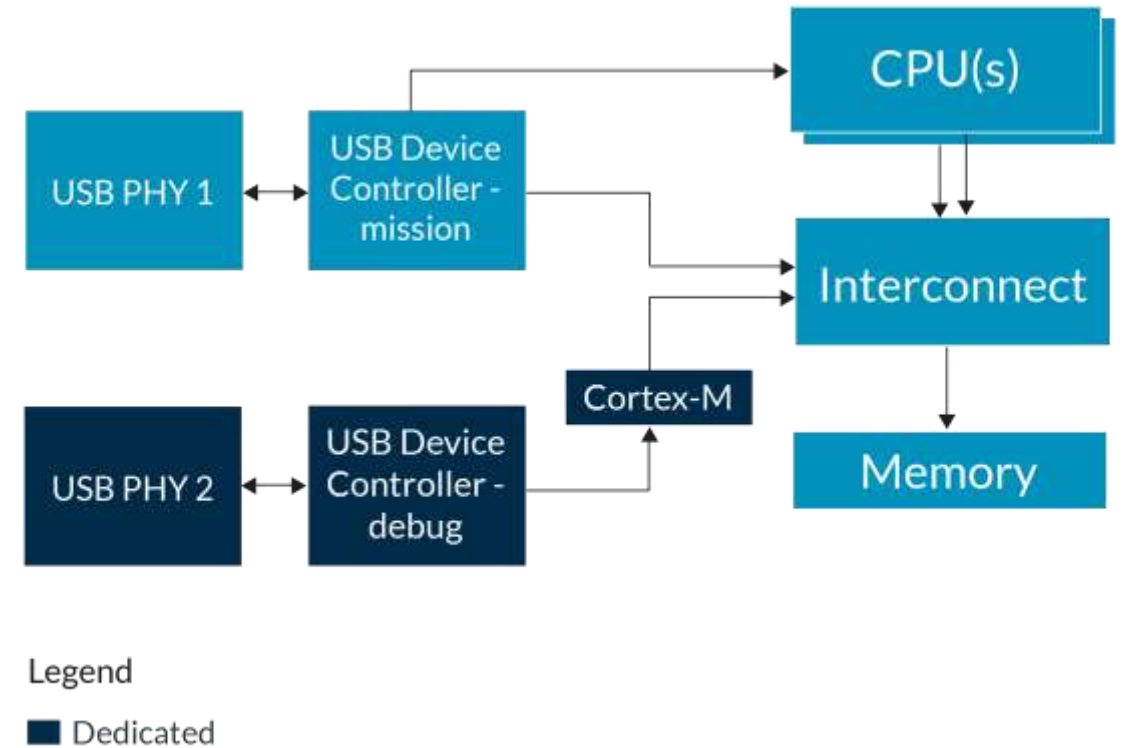


A practical approach balancing cost, intrusiveness and performance (part 2)

Non-intrusive.

Full debug features, including bare-metal.

USB interface dedicated to debug.

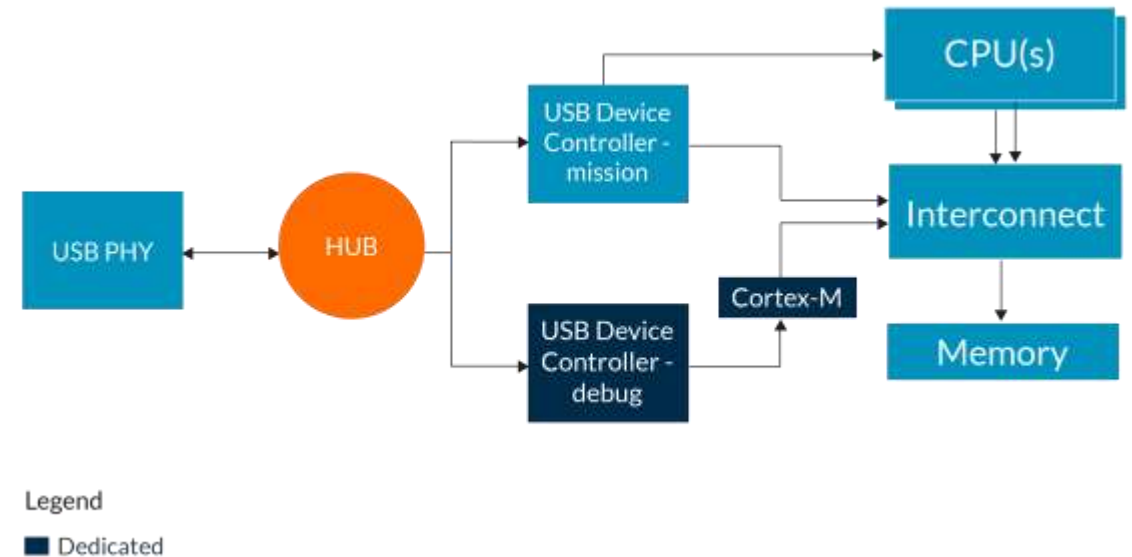


A practical approach balancing cost, intrusiveness and performance (part 3)

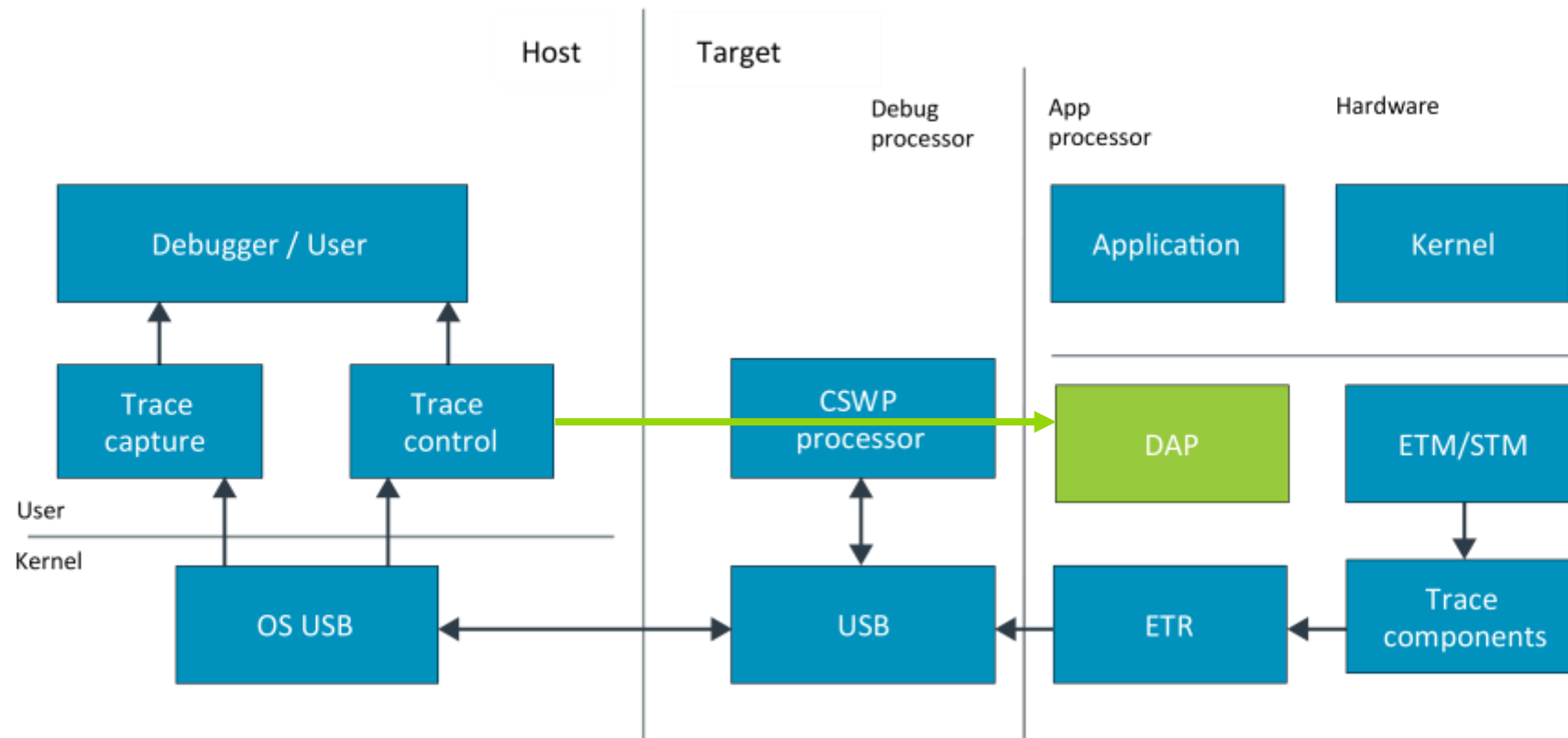
Non-intrusive.

Full debug features, including bare-metal.

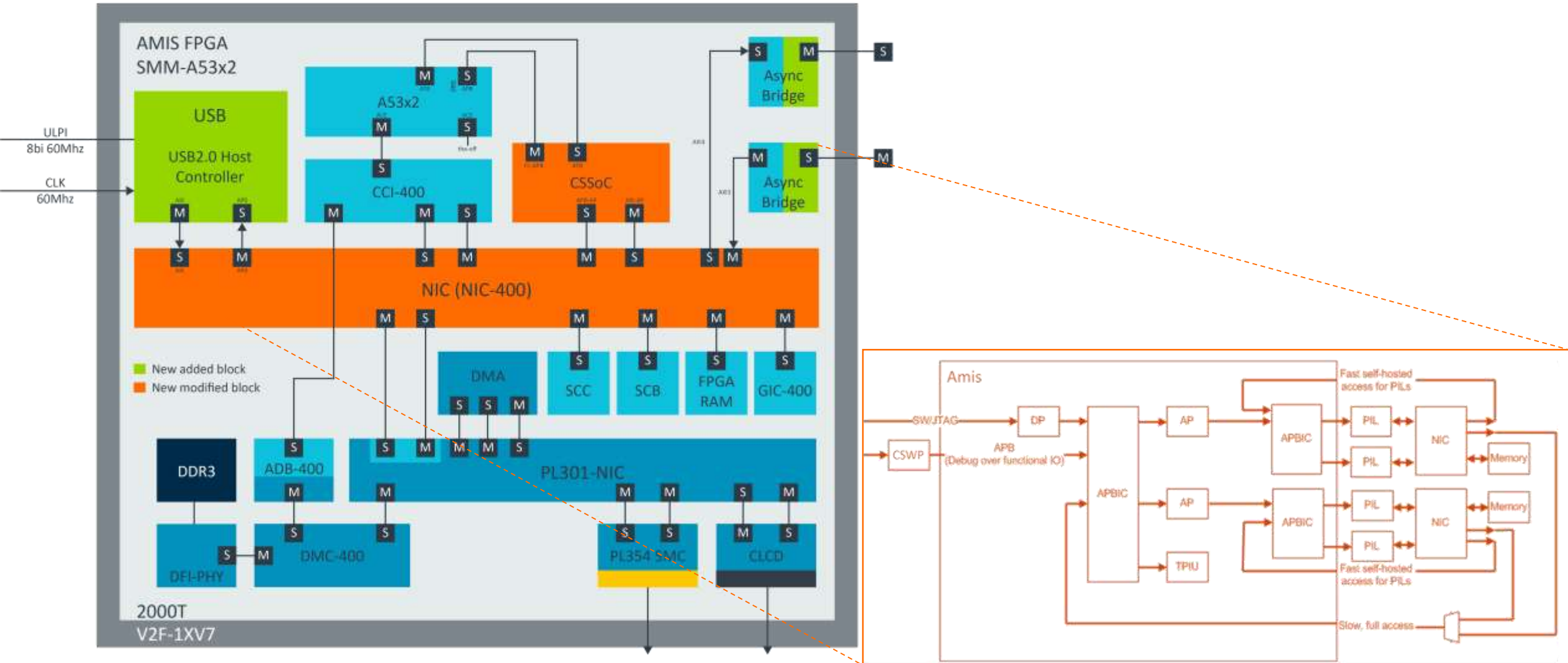
USB PHY interface shared between system
and debug.



Bare-Metal – software view



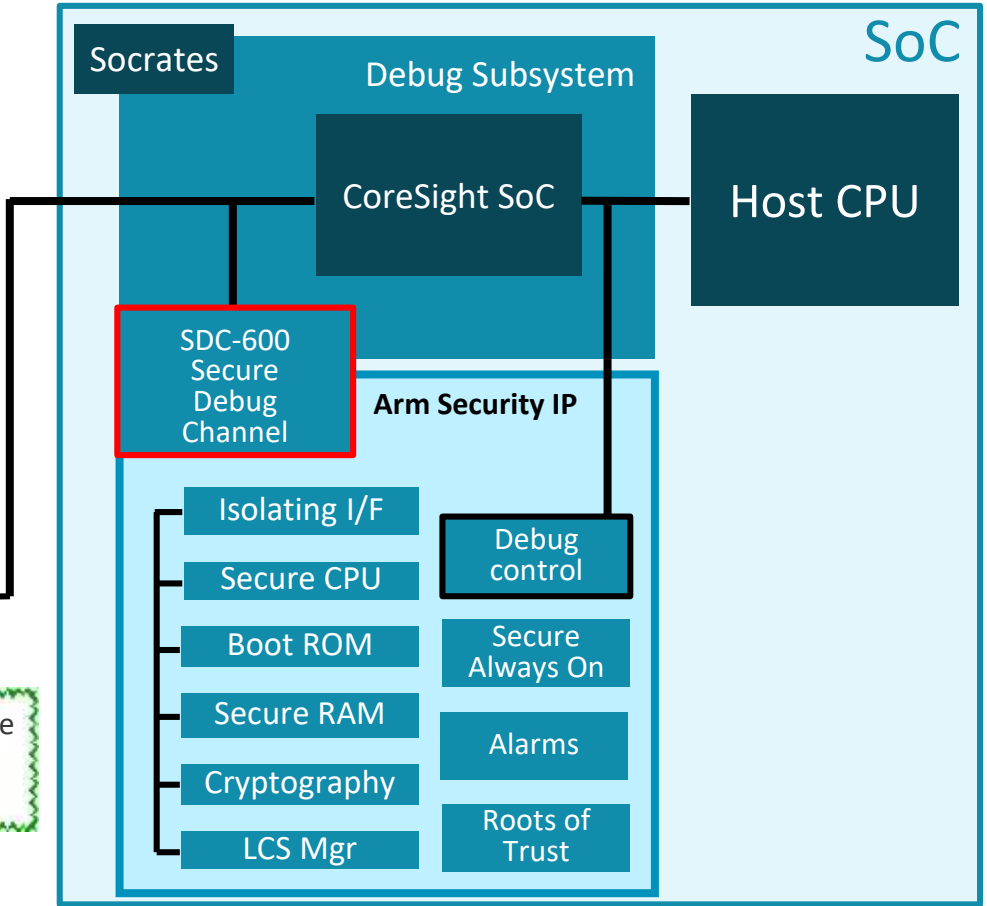
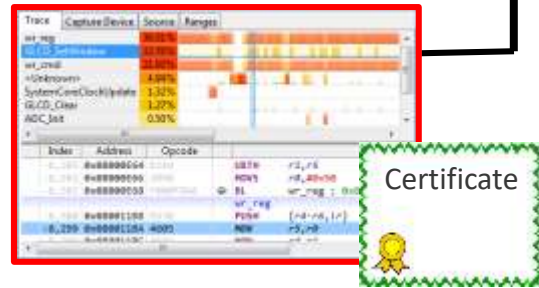
SoC-600 in FPGA



Turn-key solution for authenticated debug

Interoperability with other Arm components:

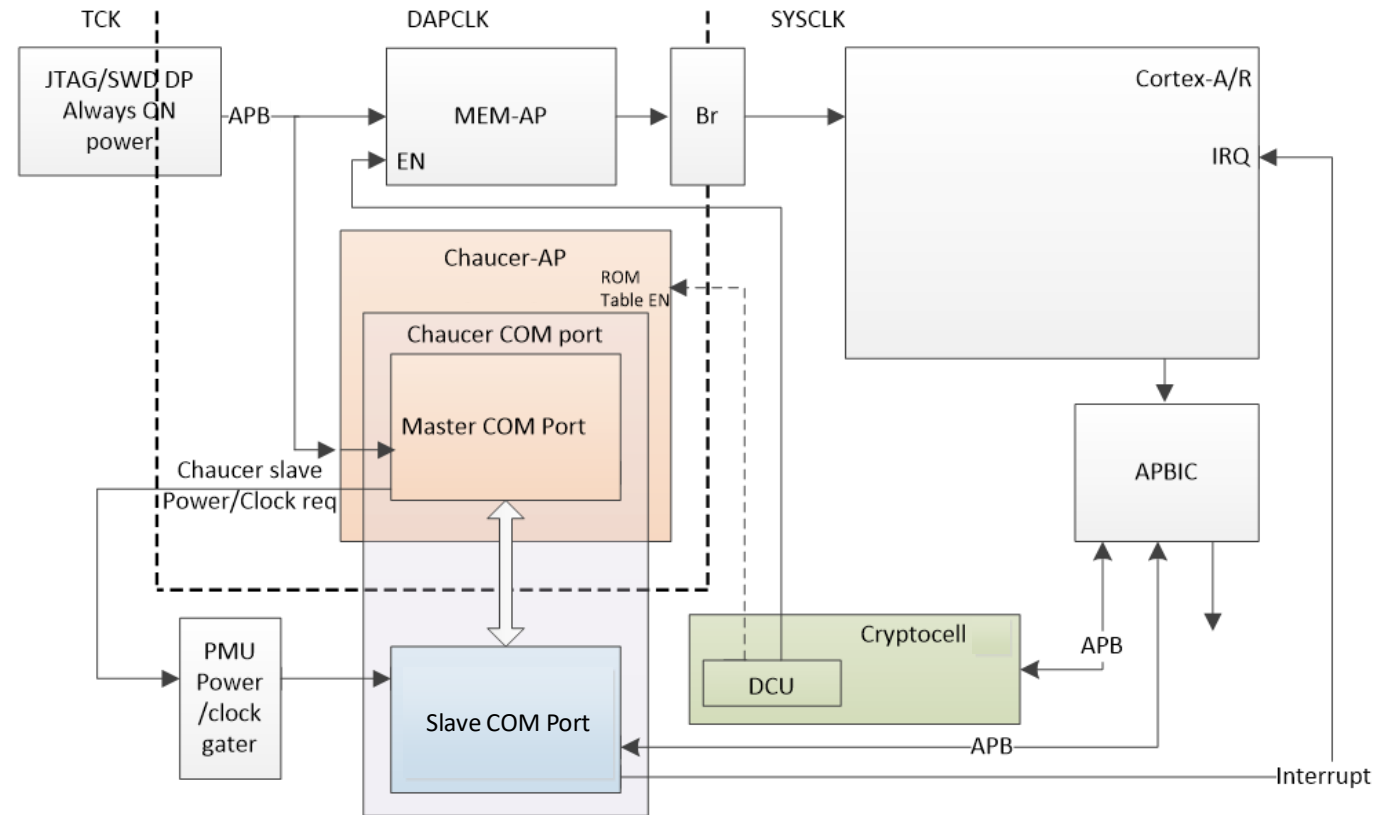
- SDC-600 (Secure Debug Channel)
 - Dedicated path to security IP
 - Standardized communication protocol
 - Full software interoperability with Arm security IP
 - Secure authentication of debug access
- Tooling support
 - Arm Socrates
 - Arm Development Studio



SDC-600 in details

Direct APB interface from DP to SDC-600.

Authentication method through SDC-600 configures access status of MEM-AP to debug memory.



CoreSight: a comprehensive end-to-end solution

IP library & tools for the creation of tailored debug and trace capabilities.

- Scales with SoC complexity from embedded design to enterprise class design

Protocol debug over any link.

- Arm provides specs and a reference implementation

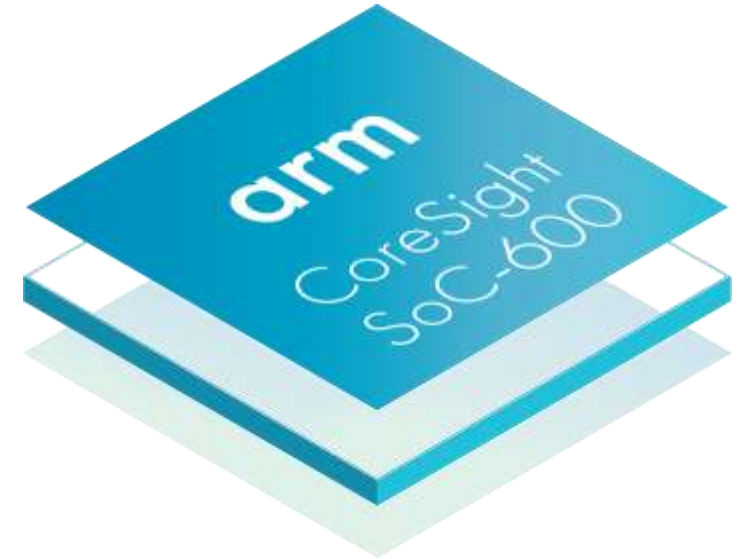
Debug tools ecosystem standardization.

- Standardized API enables any compliant debugger to support a SoC-600 based chip without HW probes

Debug access security & authentication.

- SoC-600 coupled with SDC-600 and Security IP offerings provide advanced security

Hardware PoC platform & Linux drivers.



For further information...

Find demos and more information at the Arm demo area



<https://developer.arm.com>

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Thank You!

Danke!

Merci!

谢谢!

ありがとう!

Gracias!

Kiitos!

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