A Standardized, Predictable On-chip Power Control Infrastructure

Ashley Crawford
Power Architect & Distinguished Engineer

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SoC power control requirements

Power efficient IP that participate in system level power management

- Standard interfaces for clock and power control

Power control infrastructure

- Configurable and re-usable clock and power control components
- Eliminate a time-consuming, error-prone per-project development task

Power management coordination

- Standard software interfaces
- Appropriate balance of software direction and hardware autonomy

Standard interfaces: AMBA Q-Channel & P-Channel

Component indicates activity requirement

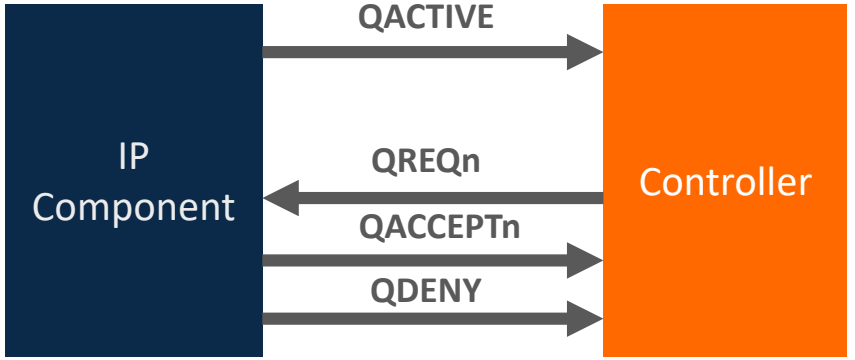
- **Q-Channel**: QACTIVE signal ➔ clock and simple power control
- **P-Channel**: PACTIVE for each mode ➔ complex power control

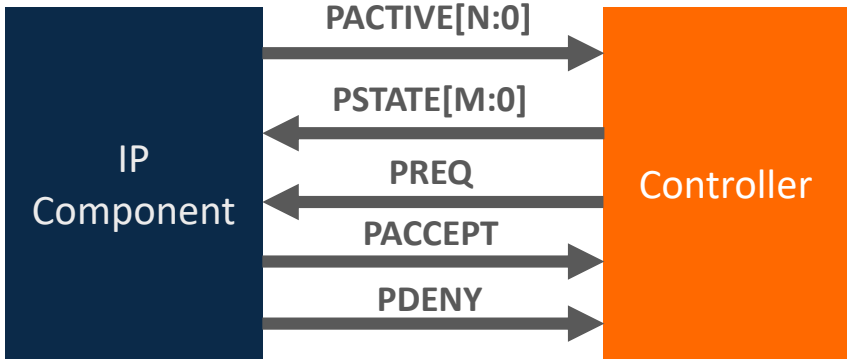
Controller requests a change in mode

- Based on xACTIVE signals, system conditions and software
- P-Channel supports multiple modes using PSTATE

Component accepts or denies the request

- According to internal conditions
- Controller completes power or clock transition





Q-Channel and P-Channel low power interface specification: http://infocenter.arm.com/help/topic/com.arm.doc.ihi0068c/index.html

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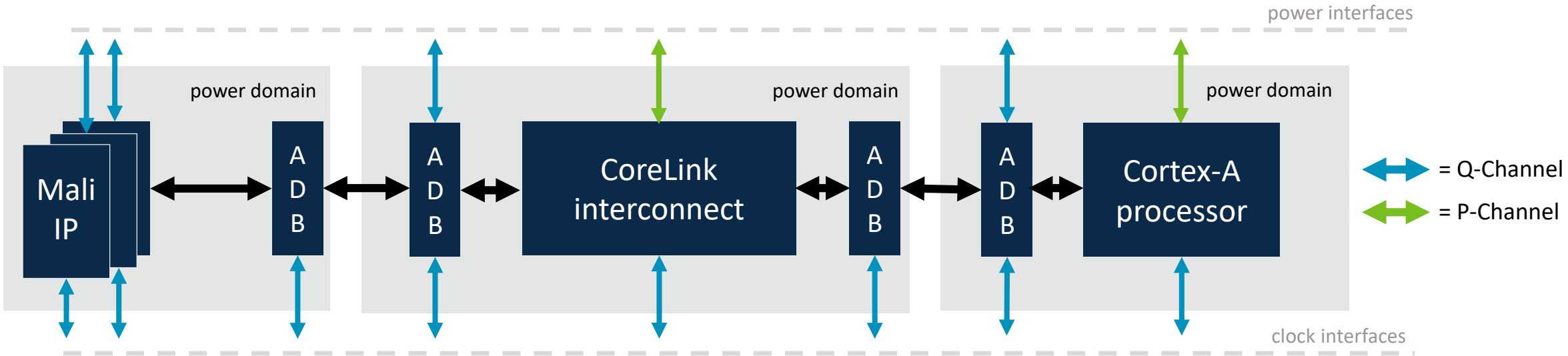
ARM IP support

Wide adoption of Q-Channel and P-Channel across Arm Cortex, CoreLink, CoreSight & Mali IP

- P-Channel implementation using standard power mode set
- ARM *Power Control System Architecture* (PCSA) provides design guidelines



Now, we need a clock and power control infrastructure…

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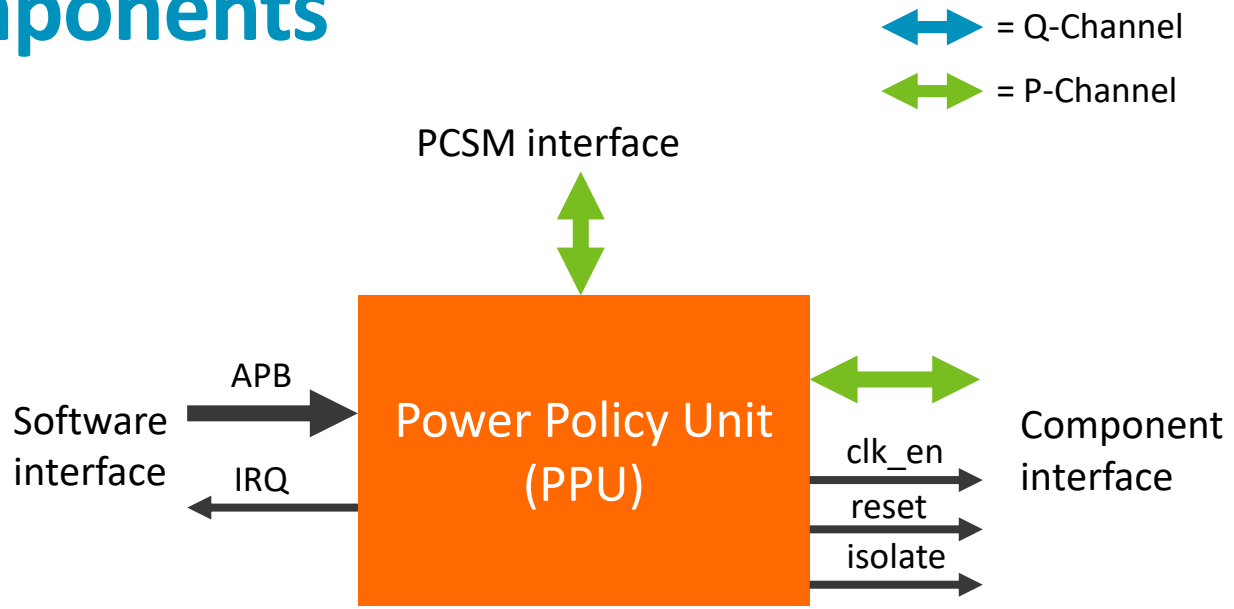
Infrastructure: controller components

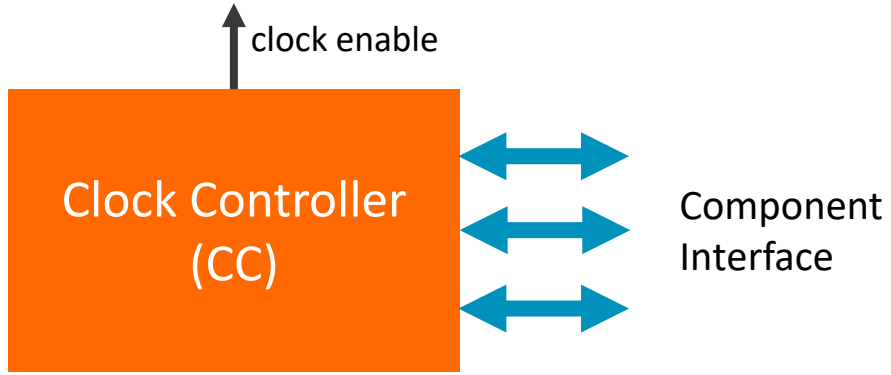
Power Policy Unit

- Highly configurable power domain controller
- Supports directed and autonomous control
- Software, component & power switch control interfaces



Clock controller

- Controller for high-level clock gating (HCG)
- Manages HCG for a single clock domain
- HCG supported by many ARM IP products



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Clock control integration

Many ARM IP support high-level clock gating (HCG) with Q-Channel

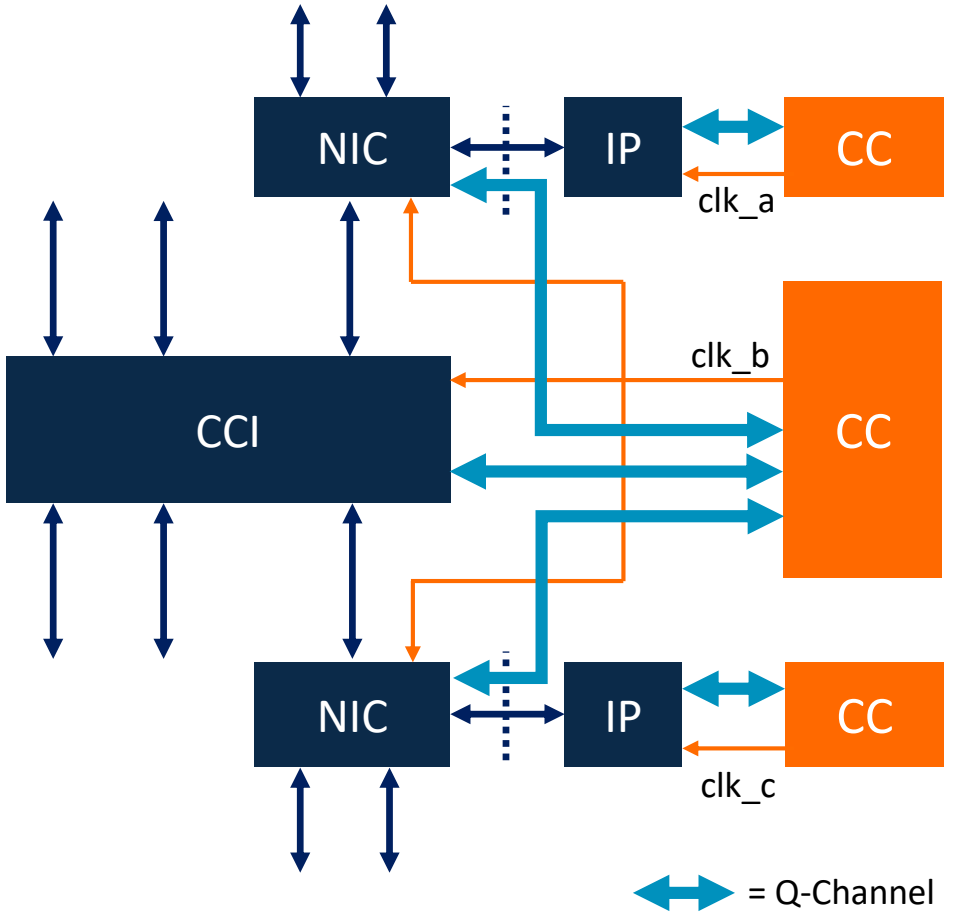
- Transaction level clock gating
- Near zero idle dynamic power
  - Gating at root of clock tree

Low power interfaces from all components in a clock domain combined at controller

- Avoids duplicate clock paths to ease clock insertion

Complementary to clock gating inside component

- HCG acts at coarser time grain



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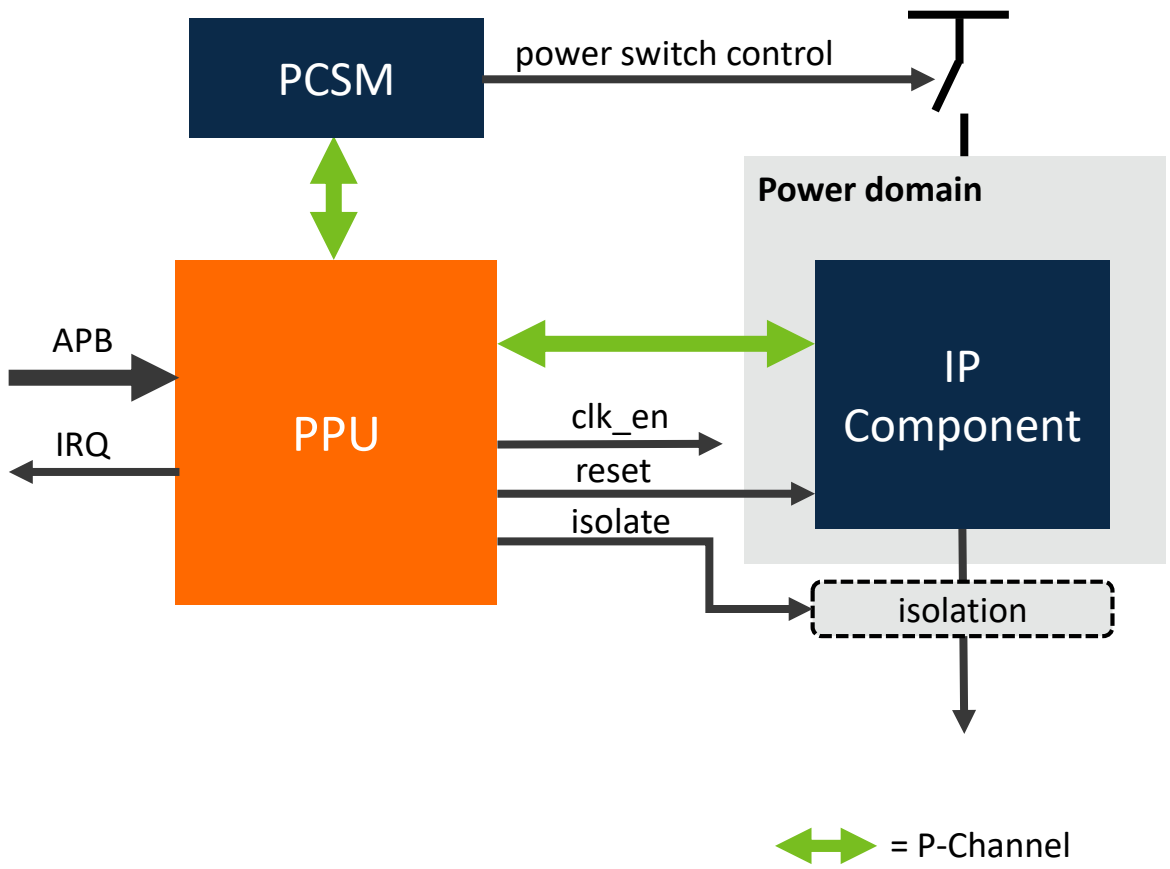
Power control integration

The PPU is technology *independent*

- Highly-configurable logical solution
- From IoT to high-end system needs
- Low-power interface (LPI) can be Q-Channel or P-Channel

Power control state machine (PCSM) is technology *dependent*

- Simple state machine specific to SoC strategy
- PPU provides a minimal P-Channel to interface the PPU to a PCSM



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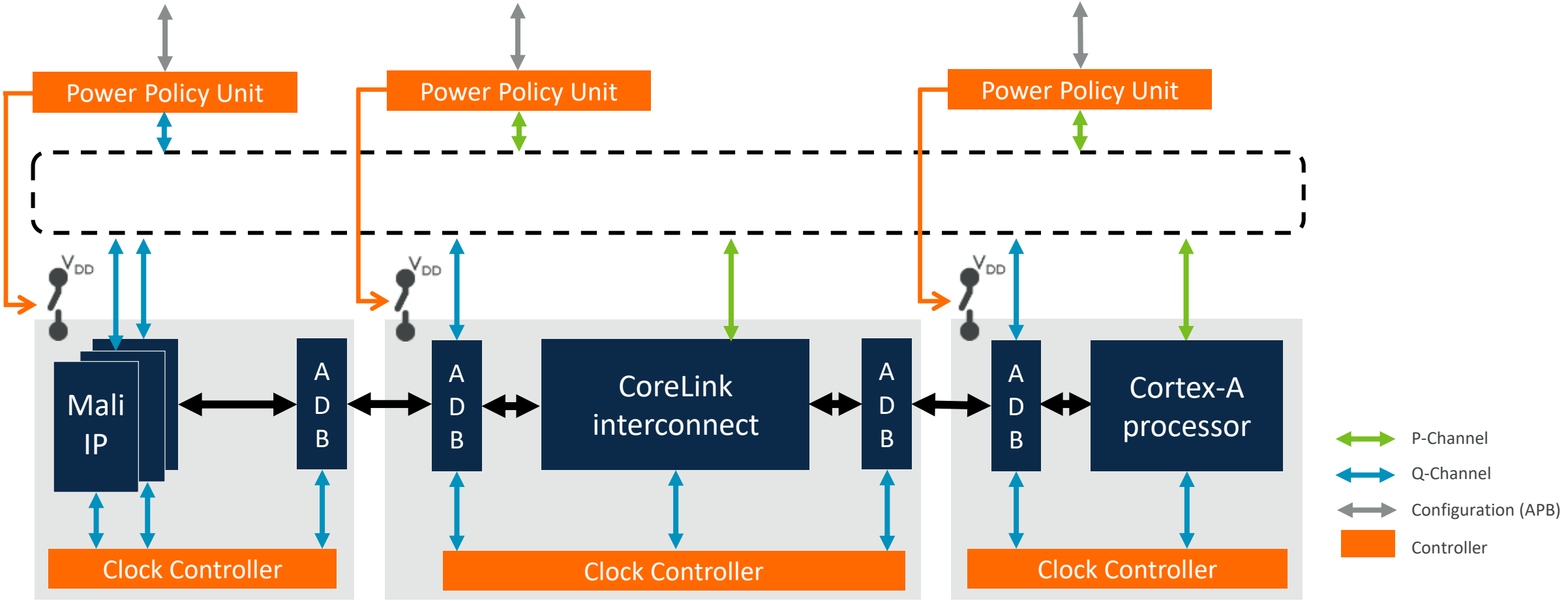
Power control infrastructure



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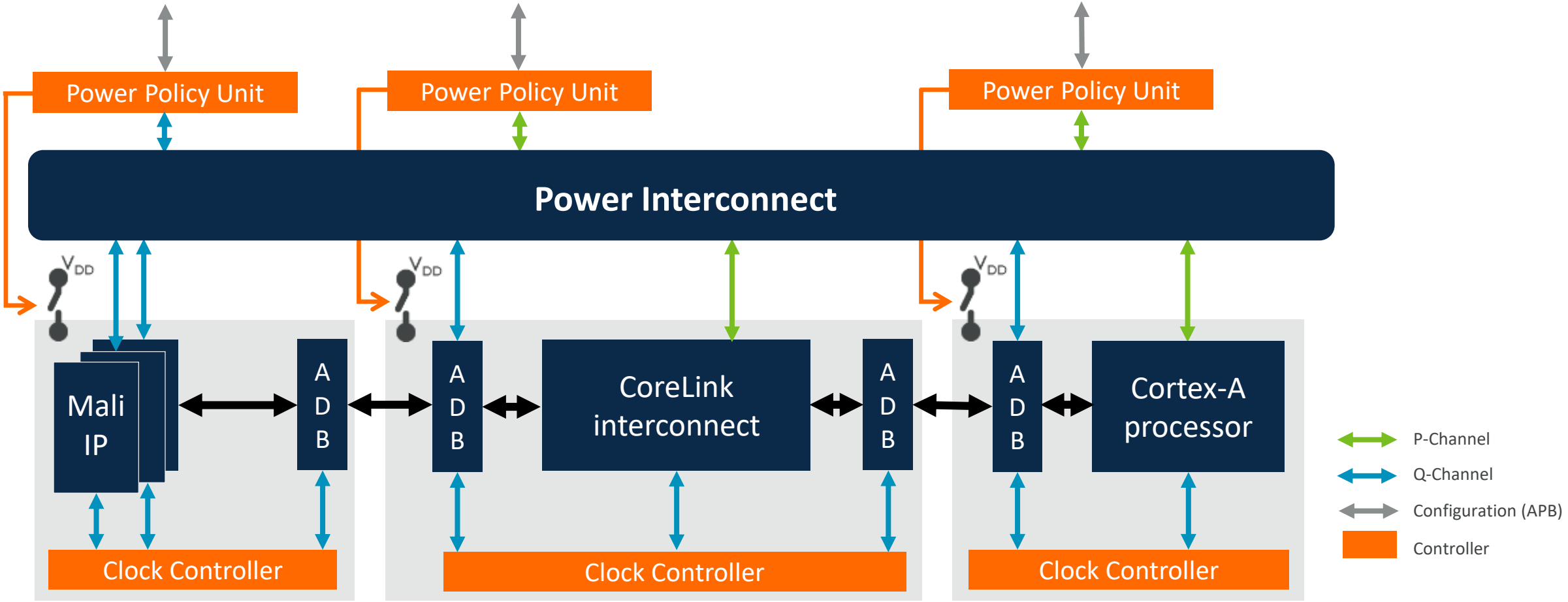
Power control infrastructure



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Infrastructure: power interconnect components

Q-Channel distributor

- 1:N fan-out from a controller to components
- Can be configured for expansion and sequencing

P-Channel distributor

- 1:N fan-out from controller to components
- Can be configured for expansion and sequencing
- Configurable re-mapping of power modes

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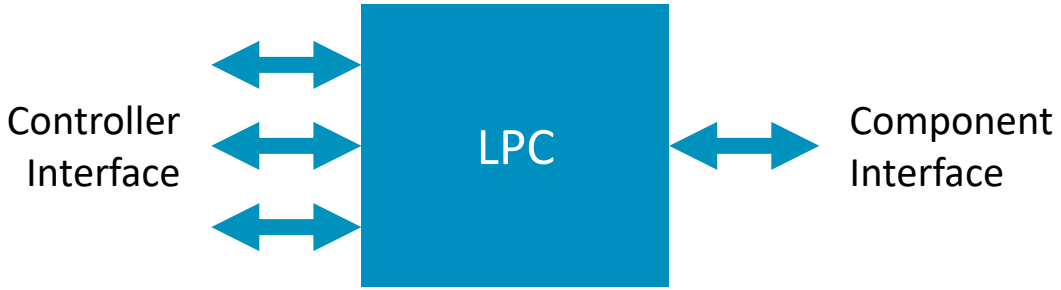
Infrastructure: power interconnect components

Q-Channel combiner

- N:1 fan-in from controllers to a component
- For control of power/voltage domain bridges
- Bridge must ‘close’ before any side powered-off
- Bridge cannot ‘open’ until both sides powered-on



P-to-Q converter

- 1:1 protocol conversion
- For integrating Q-Channel components into power domains with P-Channel PPU

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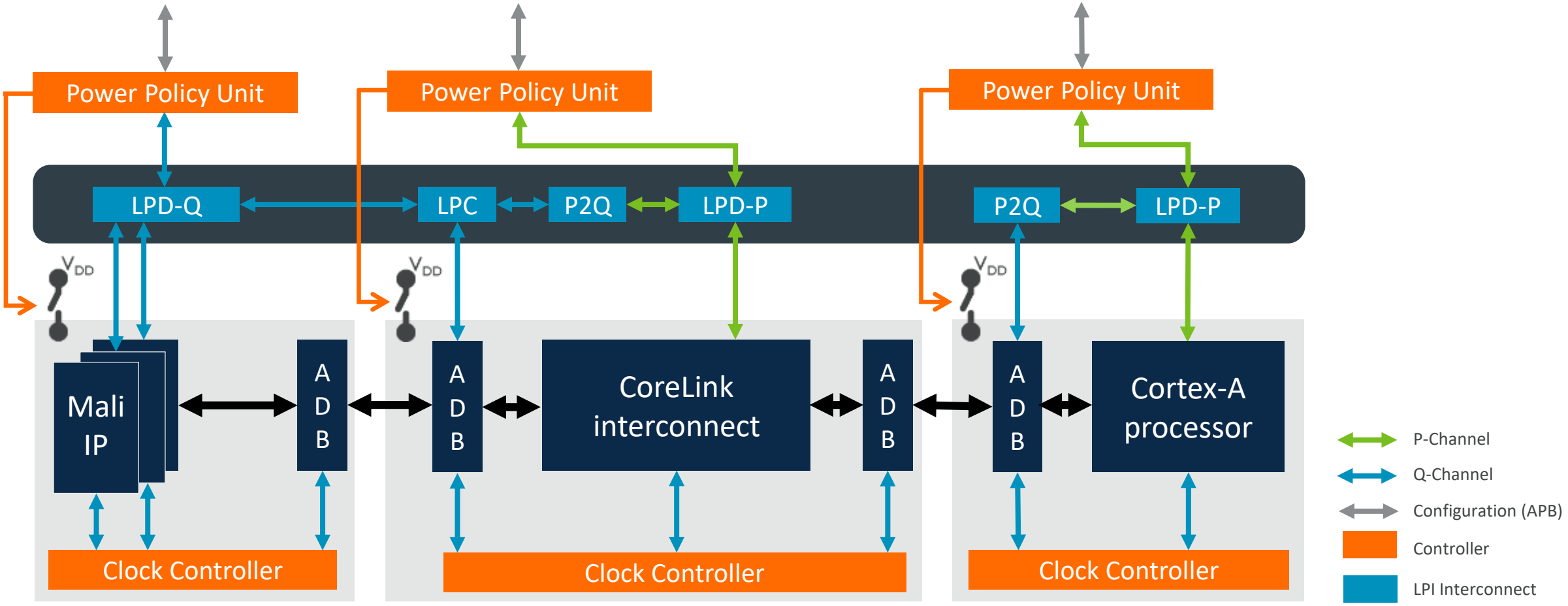
Power control infrastructure



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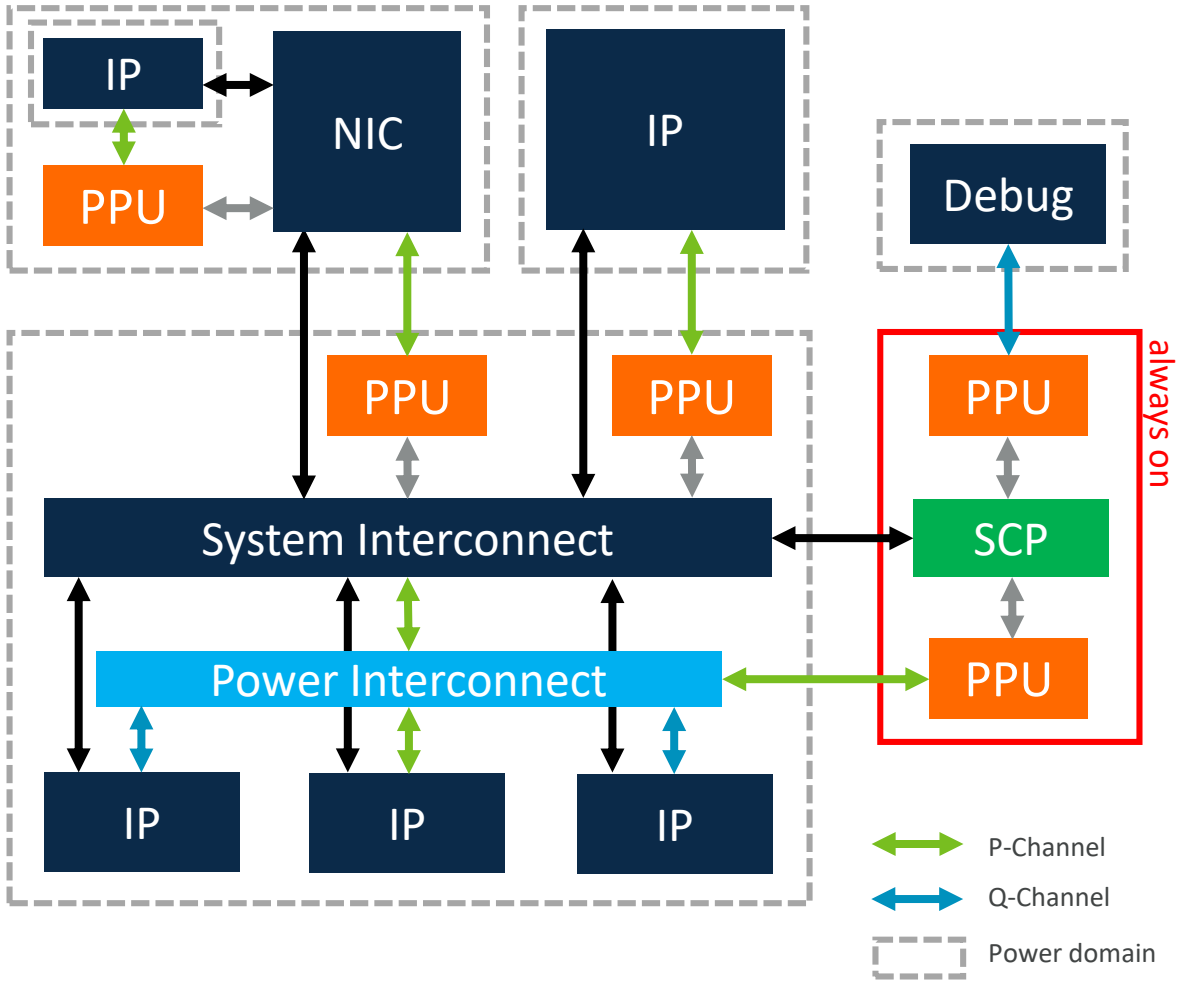
System view

Power control infrastructure is envisaged to be distributed in a complex SoC

- Functional encapsulation of SoC subsystems
- Lower latency local control for autonomous modes
- Approach used in Arm system guidance (SGM)

Coordination by System Control Processor (SCP)

- Embedded microcontroller for power management
- Arm SCMI* for commands from OS and other agents
- SCP is system aware – reconciles SW and platform constraints to select optimal policy
- Hardware assist from PPU for autonomous power transitions



* SCMI: http://infocenter.arm.com/help/topic/com.arm.doc.den0056a/DEN0056A_System_Control_and_Management_Interface.pdf

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Arm CoreLink PCK-600 Power Control Kit

Efficient Compute

Modern SoC requires multiple clock and power domains

- Management of multiple domains is complex

Optimal Power

Standardized SoC Power and Clock Management Implementation

- Implements Arm Power Control System Architecture (PCSA) guidelines
- Easing power and clock control SoC integration

Proven SoC Solution

Power and Clock Management IPs in a complete package

- Pre-verified components to accelerate time-to-market

Available early 2018

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Optimized for DynamIQ

Power and Clock Management Kit

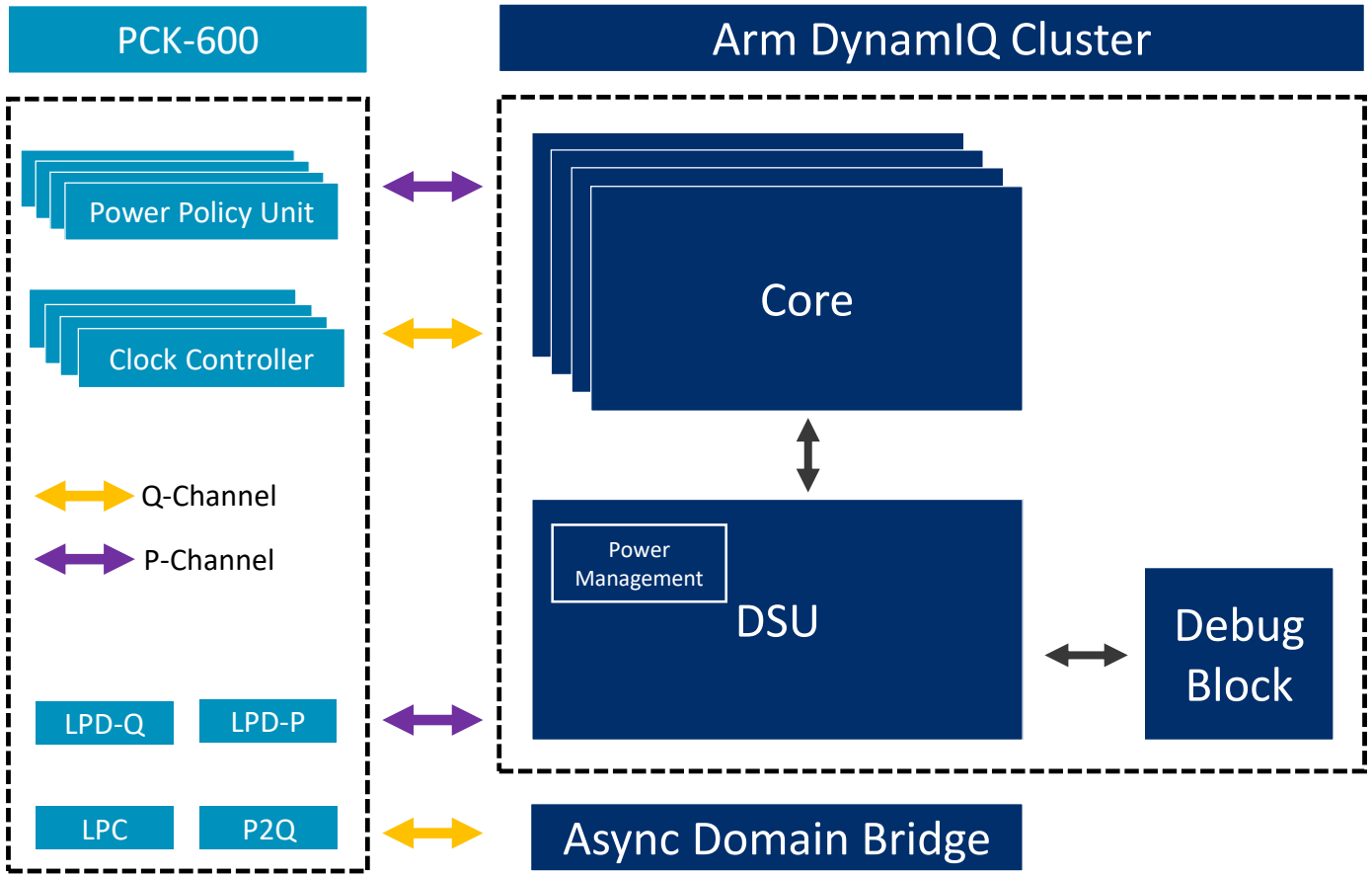
- Easing power and clock control SoC integration
- Pre-verified components to accelerate time-to-market

Compliance with Arm low power standards

- Arm Low Power Interface (LPI) architecture for interoperability with latest Arm IP
- Implements Arm Power Control System Architecture (PCSA) guidelines

PCK-600 components

- PPU – Power Policy Unit
- Clock Controller
- LPD-P, LPD-Q – P and Q-Channel Distributors
- P2Q – P-to-Q Converter
- LPC – Q-Channel Combiner



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Summary

A standardised power control infrastructure eases the path to implementing multiple power and clock domains

- Low power within the project schedule

Configurable components increase re-use and improve TTM

- Common design approach and standardised power modes
- Eases 3rd party & legacy IP integration in addition to supporting ARM IP roadmap
- Low power without error-prone project specific design work

Arm CoreLink PCK-600 power control kit available to partners in early 2018

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