Making the move from 28nm to 16nm FinFET - easy as POP

JC Yu
Technical Marketing Manager
Physical Design Group

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Agenda

- Why FinFET?
  - How can 16FFC help?
  - Differences in two technologies (planner versus FinFET)

- Implementation results using ARM’s latest core
  - ARM Cortex-A73 using TSMC 28HPC+ and TSMC 16FFC process

- Key differences between two processes for floorplanning, power planning and clock tree synthesis
  - How we make physical design easier!

- Power, Performance and Area (PPA) differences using two processes TSMC 28HPC+ and 16FFC
The new threshold for market leadership

Hisilicon, MediaTek, Spreadtrum…
…have announced plans to move to 16nm
What is a FinFET?

Traditional bulk

- Source
- Drain
- Gate Length (L)
- Gate Width (W)
- Semiconductor

3D Factor:

\[
\frac{W_{EFF,FINFET}}{W_{BULK}} = \frac{2 \cdot H_{FIN} + T_{FIN}}{F_{PITCH}}
\]

FinFET

Source
Drain
Gate Length (L)
Gate Width (W)
Standard cells and metal / fin gear ratio

- M2 pitch does not equal fin pitch
- Must consider required fin and M2 pitch
  - Yields a limited number of cell heights
  - Need integer number of fins
- Designer wants 3 active p and n fins
  - Need 2 ‘dummy’ fins between active areas
  - Need 1 ‘dummy’ fin at top and bottom boundary
- \[ 3p + 3n + 2 \text{dummy} + 2 \text{boundary} = 10 \text{ fins} \]
  - \( 10 \text{ fins} \times 48\text{nm fin pitch} = 480\text{nm cell height} \)
  - \( 480\text{nm height} / 64\text{nm M2 grid} = 7.5 \text{ tracks} \)

Note: Fin illustrations may have minor misalignments
Trends for standard cell libraries

- Generational impact (node-to-smaller node)
  - Performance: 12-track advantage vs 9-track has been decreasing
  - Power: 12-track power disadvantage vs 9-track has been very slowly declining

- Performance and library impact
  - Smaller geometries see performance gains over previous generation
  - Allows larger percentages of SoC logic to achieve target frequency with a 9-track library
  - 9-track high-density libraries still very useful
  - 7.5-track ultra-high density libraries enable area scaling

- The implication is the industry is focused on shifting to smaller libraries
Benchmarking FinFETs and ARM Cortex-A9

- **Top Frequency Comparison**
  - SC12/SC9: 1.08
  - SC10P5/SC9: 1.07

- **Power Comparison at 1GHz**
  - SC12/SC9: 1.27
  - SC10P5/SC9: 1.11

- **Power Comparison at 400MHz**
  - SC12/SC9: 1.42
  - SC10P5/SC9: 1.19

- Partial finger devices not available which significantly hurts the power signature of the larger architectures

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Minimum channel length used for all runs
Power and device tuning challenges

- **Power tuning**
  - Dynamic power is tracking VDD scaling; little or no benefit from device capacitance scaling
  - Difficult to reduce power for “slow” design
  - Limited choice for power-gated header/footer devices
  - Lack of body effect in FinFET

- **Device tuning**
  - True balanced beta ratios are not generally possible
  - Significant focus on low-power cells
  - Benchmarking shows a significant reduction in the average drive strength usage in FinFET versus planar
FinFET-based SRAM

- **Pros:**
  - Better current at same Vdd
  - Low variability (as compared to planar)
  - Lower leakage

- **Cons:**
  - Transistor width is a quantized number
  - Read disturb, write tradeoff becomes challenging

### FinFET SRAM Bit Cell

<table>
<thead>
<tr>
<th>Cell</th>
<th>No. of Fins</th>
<th>PU</th>
<th>PG</th>
<th>PD</th>
<th>Comments</th>
</tr>
</thead>
<tbody>
<tr>
<td>Cell 1: No. of Fins</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>High Variation; possible READ and Write Margin concern</td>
</tr>
<tr>
<td>Cell 2: No. of Fins</td>
<td>1</td>
<td>2</td>
<td>2</td>
<td>2</td>
<td></td>
</tr>
<tr>
<td>Cell 3: No. of Fins</td>
<td>1</td>
<td>3</td>
<td>3</td>
<td>3</td>
<td>PU variation may lead to READ Margin issue</td>
</tr>
</tbody>
</table>

- 4-5 fins needed for critical devices to reduce variations

- Variation goes up with less Fin
Implementation experiment details for ARM Cortex-A73
Advanced EDA flows and FinFET effects

ARM Artisan Power Grid Architect

Power network is critical for utilization

Double pattern typical M1 to M3

ARMARTISAN Physical IP

Synthesis/Test Insertion

Floorplanning

Placement

CTS

Routing

ATPG

Simulation

LEC

DRC/LVS/DFM

Timing Analysis

Signal Integrity

Power/IR Analysis

New Signoff Recommendations

SBOCV

Complex Power Networks

Use latest tool versions
Floorplan exploration: Cortex-A73

A73 floorplan using 28HPC+

A73 floorplan using 16FFC
FinFET challenges for power grid design

- Double pattern M1, M2 and M3
- Half-track libraries
  - Different rails for VDD and VSS
  - Sometimes V1 needs to be inserted post-route
- Pitch misalignment
- Complex DRCs
- Row end, top/bottom, and corner cap boundary cells are required

Default usage of PnR tool power grid commands will not create correct grids

- Alternate power rails are supported to optimize network based on design power density
- Upper picture: M2 totem example
- Lower picture: M2 totem with M3 or M5 strap
ARM Artisan Power Grid Architect

- **ARM Power Grid Architect (PGA)** automates critical aspects of floorplanning
  - Extremely critical for FinFET and double pattern designs
  - Useful for complex power grids in 28nm
- **Considers ARM recommended structures and ARM Artisan Physical IP**
  - Insert power grids and power gates
  - Stitch together power gate sleep signals
  - Insert boundary finishing cells as needed
  - Detect orphan row or placement site violations
- **PGA runs on industry standard floor planning tools**

Example of power network with power gating
Special library cells – boundary finishing cells

- Boundary finishing cells included to support design rules for block edges
  - **A = CNR CAP**
    - Placed in outer corners of a block
  - **B = INCNRCAP**
    - Placed at inside corners of an L-shaped block
  - **C = ENDCAP**
    - Placed at the ends of rows
  - **D = TB CAP**
    - Placed above and below the top and bottom rows of a block

- Placement options:
  - By designer using code snippets in user guide
  - By ARM Power Grid Architect
ARM POP IP – clock tree synthesis

- Choosing the optimal clock-tree components – BUF vs INV, driving strength
  - Use INV cells, not BUF cells
  - Use the lowest $V_T$ and shortest channel length available
- Clock nets NDR guideline – width and spacing
- Guidelines for routing layers, shielding, max. transition
- Recommendation for buffer drive strength, VT selection and channel length
- CTS based on MCMM analysis
Routing guidelines

Do

- Use the placement and routing options contained within ARM Tech
  - TCL files for ICC and EDI
- Use the latest versions of the tools in most cases
- Carefully design power grid for optimal routing
- Complete placement of design including FILLer cells before routing

Do not

- Do not route on M1
  - M1 outside of pin shapes can cause unfixable double-pattern violations
- Do not route using wrong-way routing on double pattern layers (M2/M3)
  - Okay for router to use small wrong-way jogs

Staggered pins for horizontal M2 route access
16FF signoff overview

ARM recommendations are consistent with TSMC recommendations

- Control over-margining; address variation
  - Signoff with SBOCV derates
  - No more using a single OCV value for a design

- SBOCV* accounts for local variation
  - Per cell derate values
  - Based on path depth and PVT corner
  - Variation decreases as path increases
  - Variation increases as voltage decreases

- Standard signoff corners
  - Setup+Hold: hot+cold SSGNP+SBOCV*
  - Hold only: hot+cold FFGNP+SBOCV*

- Stage-based OCV (SBOCV) tables
  - Derate tables go in a side file
  - Four tables for each cell: early, late, rise, fall

- Statistical Hold Constraint Margin (SHCM)
  - Includes local variation margin in hold and recovery constraint tables in the Liberty model
  *SBOCV requires using SHCM or additional margin for hold

Variations at Nominal Voltage

- Temperature ~1%
- Voltage ~42%
- Process ~57%

Variations at Low Voltage (Vnom-20%)

- Temperature ~2%
- Voltage ~58%
- Process ~40%
What is POP IP?

- Includes all ARM Artisan Physical IP products that are required to build a processor
- ARM POP IP assists you in rapid product development by minimizing the Time to Market (TTM) and achieve best-in-class
  - Performance
  - Power
  - and Area (PPA)
- ARM POP IP does not provide RTL deliverables
- Customer can configure the RTL and use ARM POP IP deliverables during the implementation phase of design
Summary

- Moving from TSMC 28nm to TSMC 16nm FinFET can be done easily:
  - 9 track or 10.5 track architecture for standard cells gives similar performance vs. 12 track
  - For easier power grid creation and DRC fixing, use ARM’s Power Grid Architect
  - Inverter usage is recommended for clock tree synthesis
  - Use ENDCAP cells to meet DRC requirement at 16nm
  - Signoff with SBOCV derates

- Artisan POP IP for Cortex-A73 on TSMC 16FFLL+ achieves 3GHz frequency for mobile applications