Accelerating infrastructure SoC time-to-market

ARM

Mario Cooper
Senior Product Manager

ARM Tech Symposia China
October 31 – November 4, 2016

Accelerating your SoC design

What?

This session will focus on system level work ARM is doing and how it can help partners to accelerate their SoC designs

Why?

Time to Market is critical to successful product introduction. Even if product is similar to other products, getting there first can mean difference between success and failure

How?

Leverage IP blocks that have already been completed, tools that can generate RTL quickly, and fast models to jump start software stack development

Deploy systems in less time

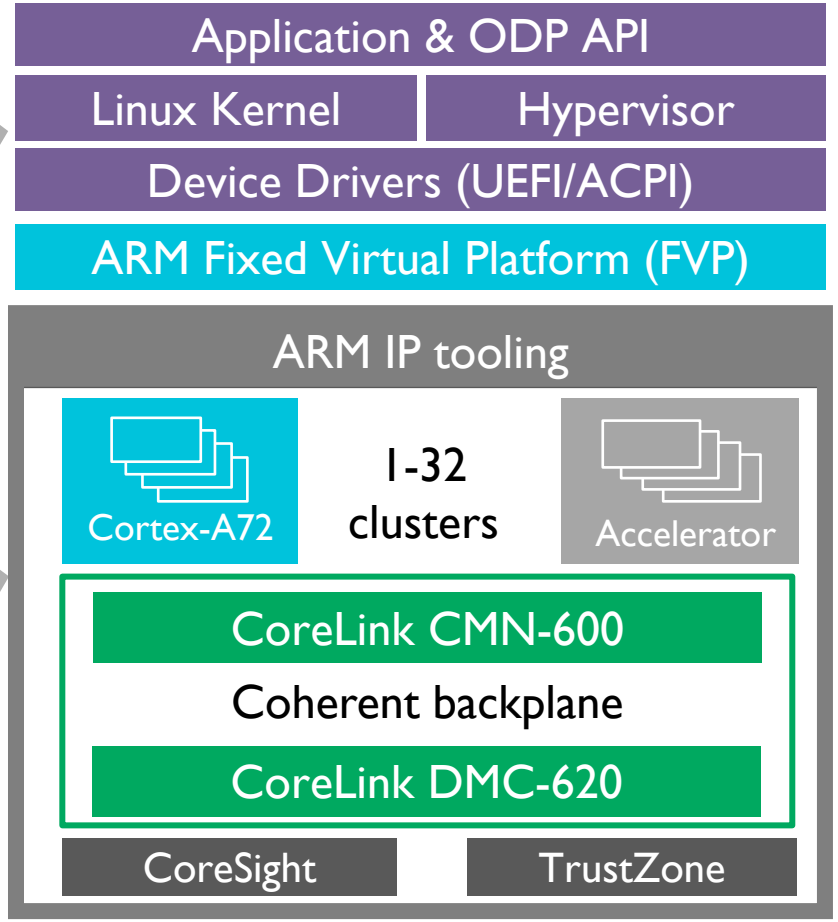
Accelerate software deployment

- Open source device drivers for CoreLink IP
- Start system prototyping with ARM Fast Models and Fixed Virtual Platforms

Jump start SoC designs

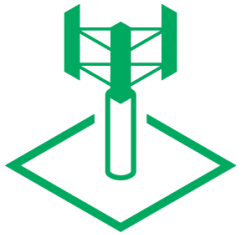
- Peta cycles of system validation
- Measured RTL industry benchmark reports
- Measured area and power in targeted process nodes

Reference Data



ARM

What is Reference Data?



Infrastructure

Subsystems

Software

- Reference Data is a collection of resources to provide a representative view of typical compute subsystems that can be designed and implemented using current and future ARM IP releases

- Reference Data comprises:
  - Documentation set
  - Fixed Virtual Platform (FVP)
  - Integrated software stack

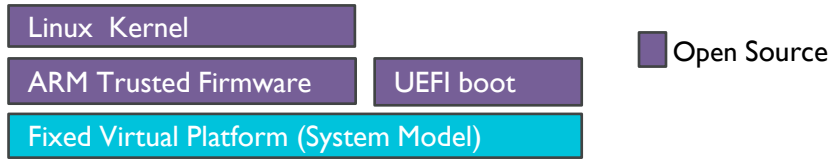
Reference Data deliverables

Bill of Materials

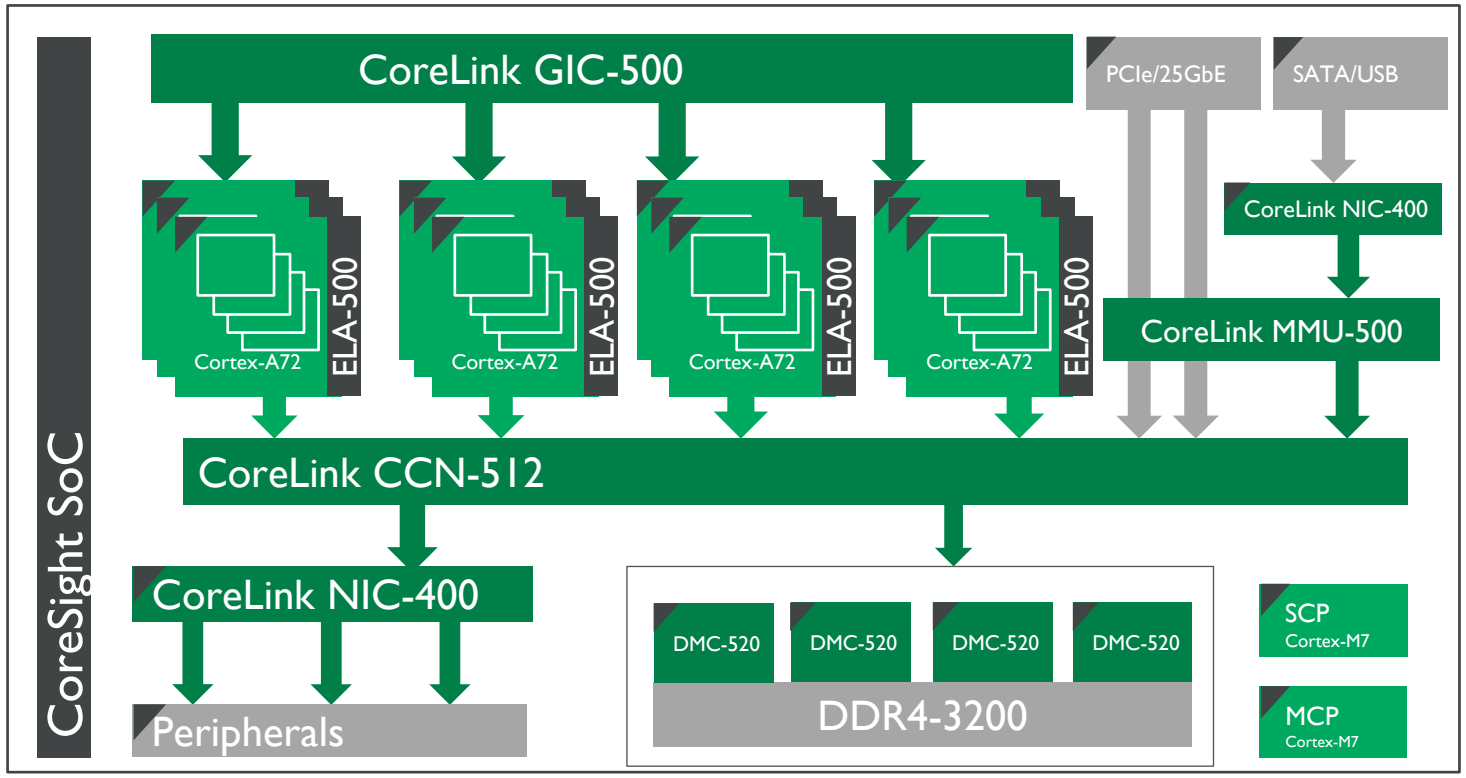
- Documents
  - System Design Presentations
  - Technical Overview
  - System Analysis Report
  - Implementation Guidelines
  - FVP Programmers Guide
  - Software Release Notes
- Fixed Virtual Platform
- Software
  - Build scripts and patches for Open Source

- Delivery Mechanism
  - Freely available – contact your partner manager
  - New Connect DropZone
  - Click through licensing
  - FVP available through existing channels
    - Licensing through ARM
    - Free version available through
    - https://developer.arm.com/products/system-design/fixed-virtual-platforms
  - Linked to projects available in Fast Models

Reference Data example



- Target low-to-mid range infrastructure solutions
  - Reference data for 2017 solutions
- ARMv8-A hardware
  - Server Based System Architecture (SBSAv3)
  - 48x Cortex-A72 or 24x Cortex A53
  - Up to 32MB L3 cache
  - Up to 4x DDR4-3200 (DMC-520)
  - Up to 18 AXI expansion ports
  - I/O Coherent PCIe, Ethernet, Offload
- Software stack
  - Standard Platform interfaces with ARM Trusted Firmware
  - Linux Kernel



ARM

Reference Data outputs

- System design
  - Describes architecture explored to achieve Performance, Power, and Area targets
- Technical overview
  - Detailed description of the reference subsystem Hardware and Software components
- Implementation guidance
  - Documents and describes reference subsystem level physical implementation work and trials
- System analysis report
  - Documents the reference subsystem RTL emulation performance results
- FVP implementation guide
  - Describes the reference subsystem memory mapping and registers

Reference Data examples

HW and SW overview – config1 (Cortex-A72)

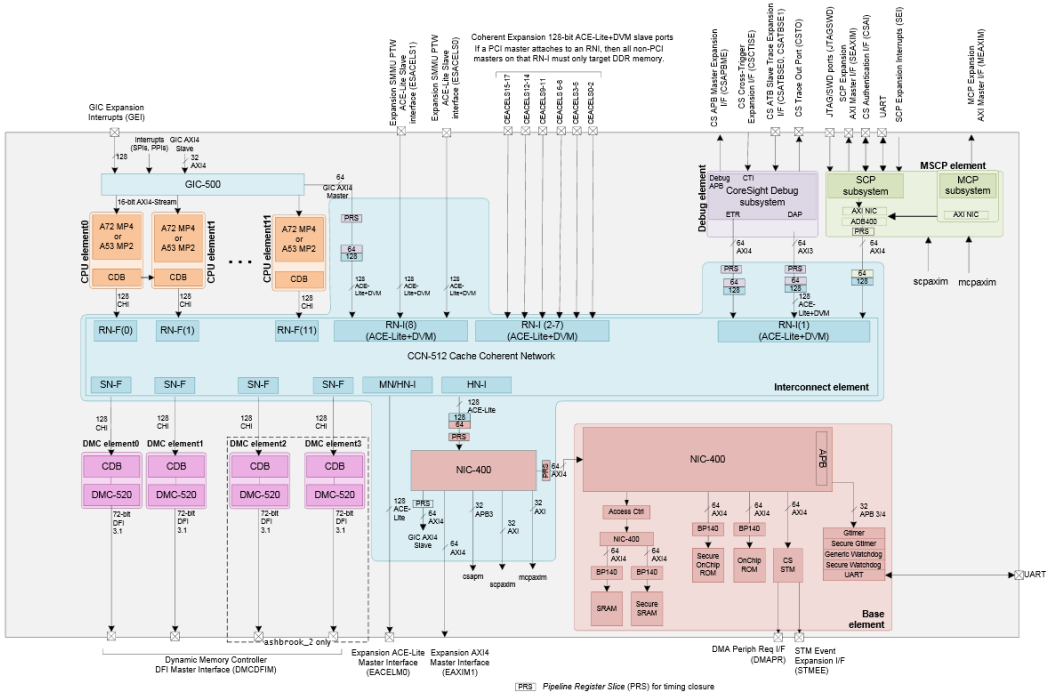
Targeting mid-range servers and base stations

- ARMv8-A subsystem design for infrastructure
  - Server Based System Architecture v3.0
  - 48(12 xMP4) Cortex-A72 processors
  - Large 32 MB L3 system level cache
  - 4 * x72/x40 DDR4-2667/3200
  - Multiple ACE-Lite + DVM expansion ports for:
    - I/O Coherent PCIe, Ethernet, Offload, and so on.
  - Cortex-M7 for SCP and MCP
- Software stack from ARM Trusted Firmware to Linux
  - Advanced power & thermal management
    - SCP firmware binaries - power, thermal and system control
    - MCP firmware binaries - manageability, RAS and event logging control
  - ARM Trusted Firmware platform port build on open source base
  - UEFI/ACPI platform port
  - Linux Kernel

System partitioning

The Reference Data design partitions the system into functional blocks, also known as *elements*.

- The following figure shows a block diagram of the elements that the FVP models.



CPU element: Contains an application processor, associated logic for debug and the control of clocks, reset, and power. The Reference Data has 12 CPU elements that all contain a Cortex-A72 processor or a Cortex-A53 processor.

Interconnect element: Contains a CoreLink CCN-512, several CoreLink NIC-400, and a CoreLink GIC-500. The NIC-400 interconnects provide master and slave extension interfaces so that you can connect your masters and slaves to the Reference Data.

DMC element: Contains a CoreLink DMC-520 *Dynamic Memory Controller* (DMC) and associated logic for debug and the control of clocks. A Cortex-A53 Reference Data has two DMC elements and a Cortex-A72 Reference Data has four DMC elements.

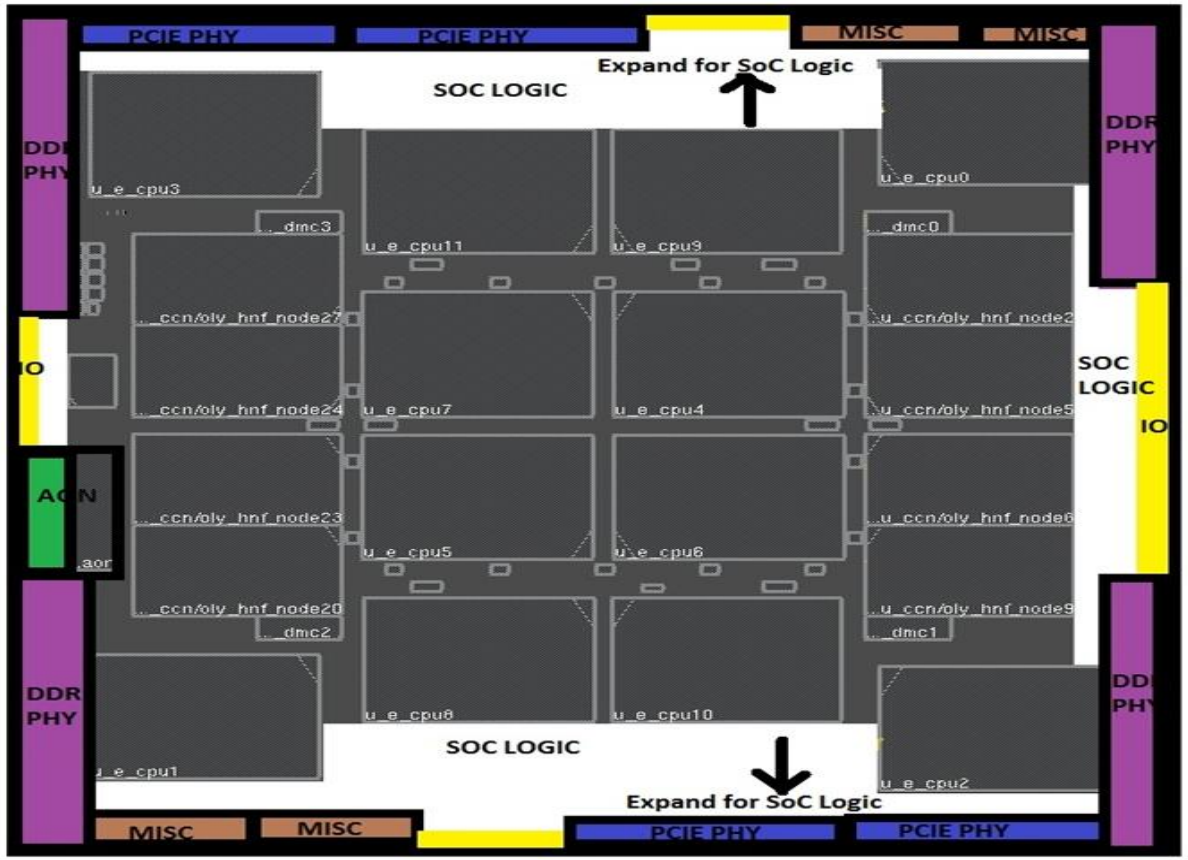
Base element: Implements all peripherals that the Reference Data design requires.

MSCP element: Contains a *System Control Processor* (SCP) block and a *Manageability Control*

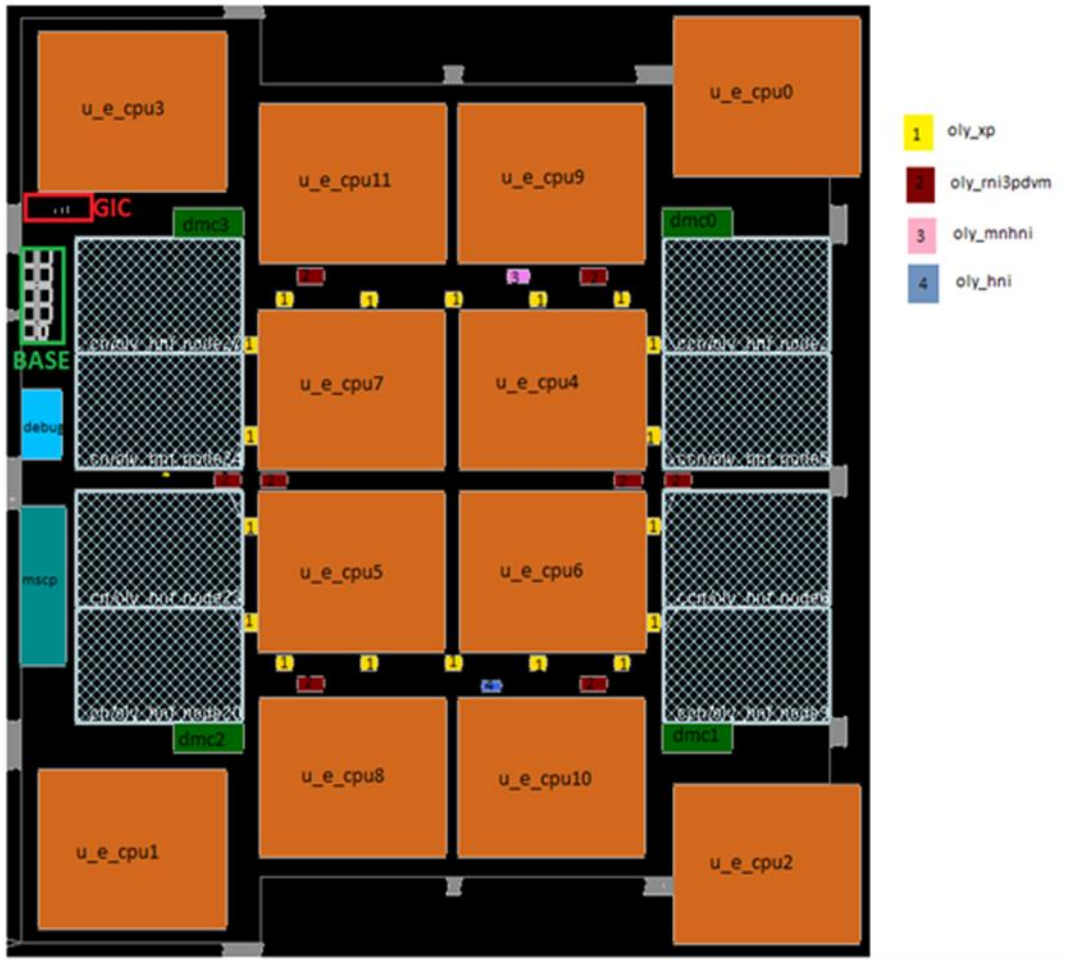
Debug element: This reference design implements the CoreSight-based debug subsystem.

Representative floorplans

SOC floorplan mock-up



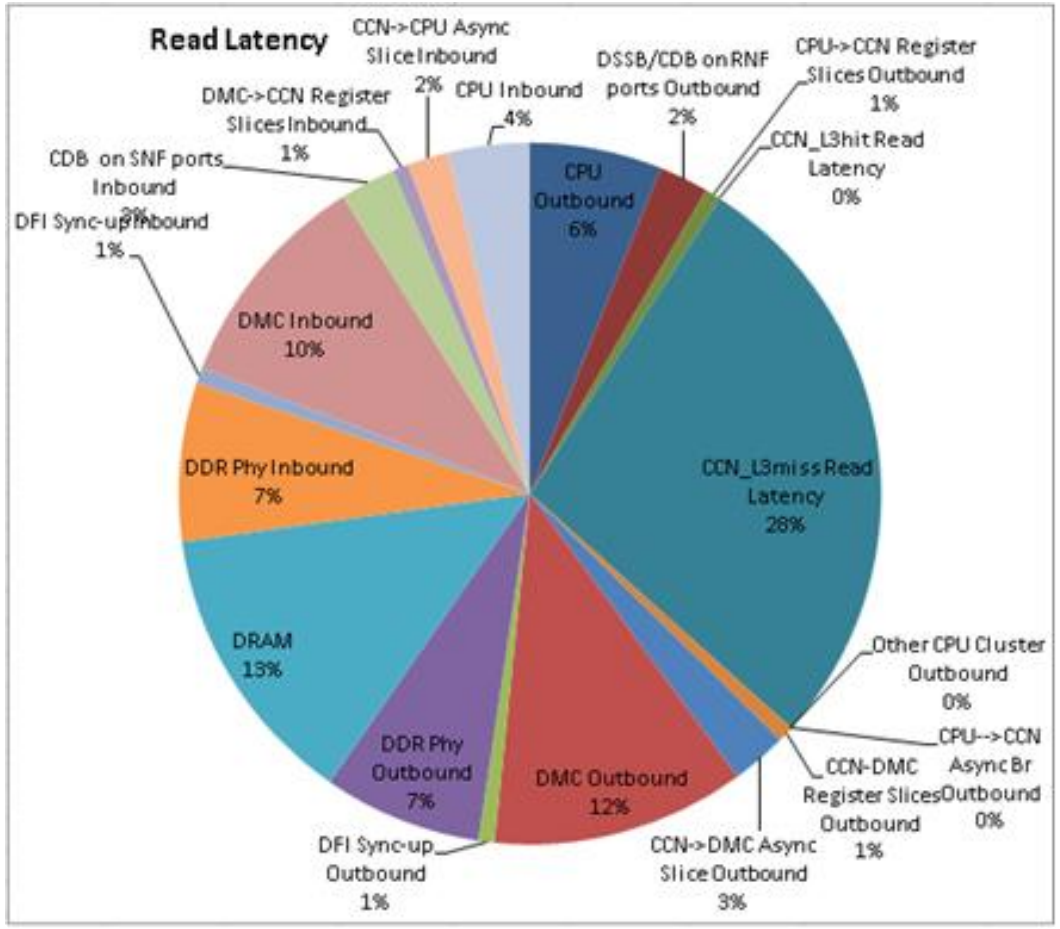
Reference design floorplan



ARM

Processor read latency

Processor read latency for Open Row DRAM



ARM performance characterization work helps you lock down your SOC design quicker

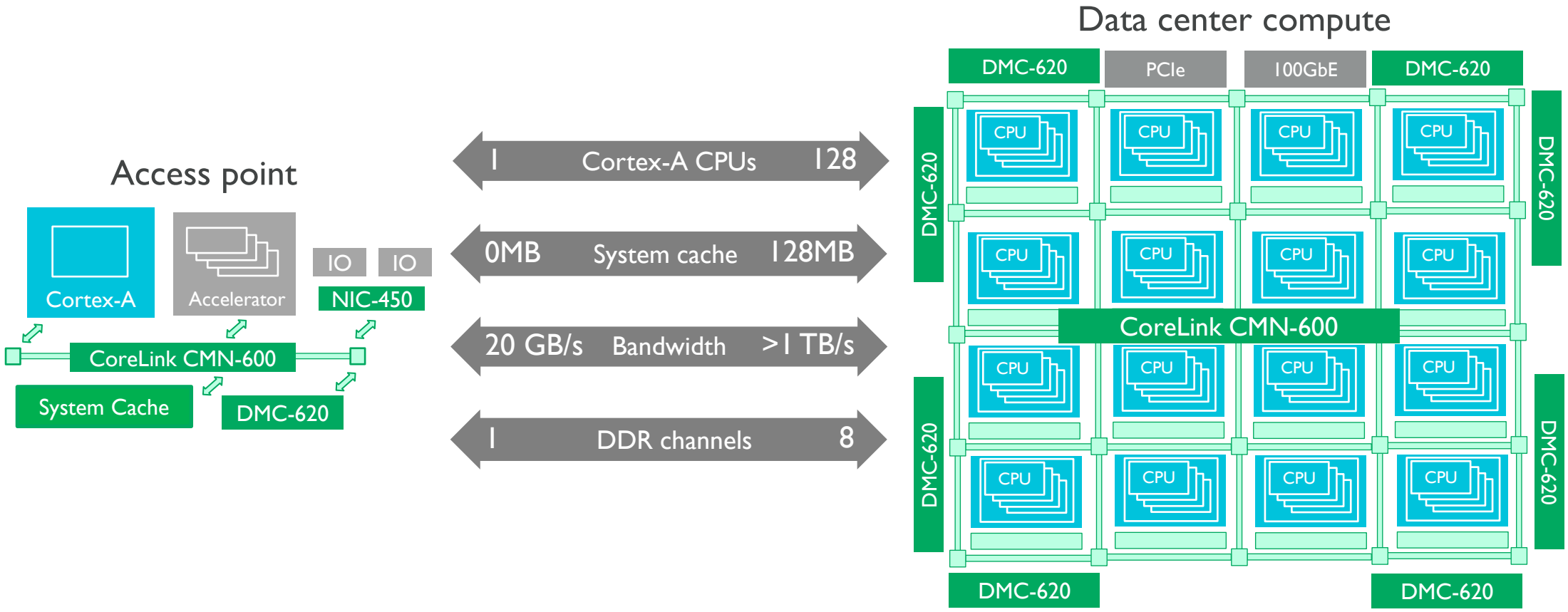
Reference Data FVP

The Reference Data FVP models multiple IP components

- The FVP models the following IP components:
  - Twelve MP4 Cortex-A72 processors or 12 MP2 Cortex-A53 processors
  - A *System Control Processor* (SCP) that is based on the Cortex-M7 processor
  - A *Manageability Control Processor* (MCP) that is based on the Cortex-M7 processor
  - A CoreLink CCN-512 Cache Coherent Network
  - Multiple CoreLink NIC-400 Network Interconnects
  - Memory access path towards DRAM
- The Reference Data FVP drives:
  - System architecture and software standardization
  - Provides software and binaries of proprietary firmware

Summary

New Reference Data examples coming soon

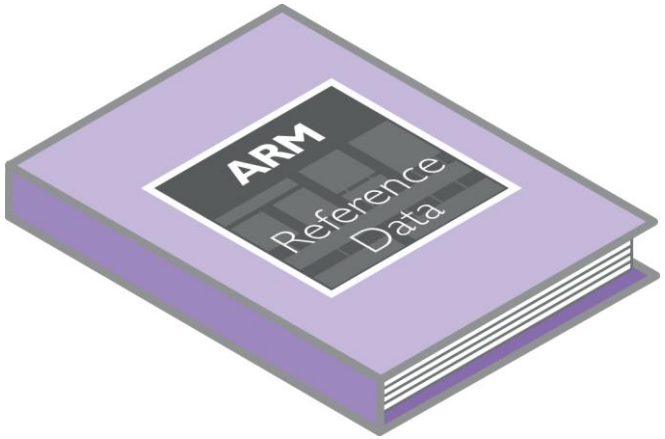


3rd generation ARM coherent backplane IP optimized for performance and scale

CoreLink CMN-600 and CoreLink DMC-620

ARM

Reference Data – faster path SoC to market



- Reference Data provides free additional information to help customers design large infrastructure SoCs
- Comprehensive set of data helps you develop your SoC faster with less risk
  - Quickly assess performance targets to lock down your design quicker
  - Confidence that ARM IP works well together
  - HW and SW guidelines, open source patches
- Leverage ARM system design key learnings
  - Large SoC integration challenges and performance analysis
  - Focus your efforts on differentiation

Deliver SoC months earlier

Leverage ARM learnings

Questions?
Want to know more?
Please contact mario.cooper@arm.com

ARM